Digital Delay Generator Model 7085

INSTRUCTION MANUAL

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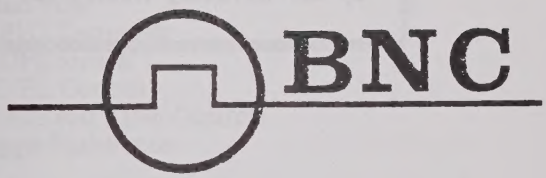


Digital Delay Generator Model 7085

INSTRUCTION MANUAL

(PRELIMINARY)

BERKELEY NUCLEONICS CORPORATION
1198 Tenth St., Berkeley, California 94710

Warranty

Berkeley Nucleonics Corporation warrants all instruments, including component parts, to be free from defects in material and workmanship, under normal use and service for a period of one year. If repairs are required during the warranty period, contact the factory for component replacement or shipping instructions. Include serial number of the instrument. This warranty is void if the unit is repaired or altered by others than those authorized by the Berkeley Nucleonics Corporation.

CONTENTS

FRONT MATTER

Title Page
Warranty
Contents
Frontispiece

SECTION 1 SPECIFICATIONS

SECTION 2 OPERATING INFORMATION

2.1 General

2.1.1 Power-Up
2.1.2 Performance Information
2.1.3 Operating Temperature
2.1.4 Cables, Attenuators and Oscilloscopes

2.2 Operating Controls and Connectors

2.2.1 Line Voltage and 115/230 Switch
2.2.2 Power Switch and Fuse
2.2.3 EXT TRIG INPUT Connector
2.2.4 EXT TRIG SLOPE Switch
2.2.5 EXT TRIG LEVEL Control
2.2.6 TRIGGER MODE and FINE Controls
2.2.7 MANUAL Trigger Pushbutton
2.2.8 ERROR Light
2.2.9 INITIAL Output Connector
2.2.10 NORMAL AND COMPLEMENT Output Connectors
2.2.11 AMLITUDE Controls
2.2.12 EDIT Pushbuttons
2.2.13 DELAY and WIDTH Display
2.2.14 MEMory Display and Pushbuttons
2.2.15 Data Entry Keyboard
2.2.16 UPDATE Pushbutton and Light
2.2.17 NEXT Pushbutton
2.2.18 HOME Pushbutton
2.2.19 REMote ENable/LOCal Pushbutton and Light
2.2.20 SCAN Pushbutton and Light
2.2.21 NEGative OUTPUT
2.2.22 ECL/NORM Switch
2.2.23 PROGRAM IN Connector
2.2.24 ADRS/RESET MODE/ERROR OUT Switches
2.2.25 EXTernal CLOCK Connector (Option B)
2.2.26 EXTernal CLOCK 10MHZ-1MHZ Switch (Option B)
2.2.27 INITialize-STORE Switch (Option E)

2.3 Operating Instructions

2.3.1 General
2.3.2 Turn-On
2.3.3 Timing Generation
2.3.4 Memory Manipulation
2.3.5 Examples (of Timing and Memory Operations)
2.3.6 Multiple Delays and Widths

2.4 Remote Programming

2.4.1 General
2.4.2 The IEEE 488-1978 Bus (GPIB)
2.4.3 System Connection
2.4.4 Programming Data
2.4.5 Operating Considerations
2.4.6 Programming Connector

2.5 Options

2.5.1 External Frequency Reference - Option B
2.5.2 Extended Memory with Battery Backup - Option E

SECTION 3 SCHEMATICS

SECTION 2
OPERATING INFORMATION

2.1 GENERAL

This section will serve to familiarize the operator with the varied capabilities of the BNC Model 7085 Digital Delay/Width Generator. Operating controls and connectors as well as operating instructions will be covered. In this section whenever a control is discussed the front or rear panel wording will be capitalized. Consider for example: TRIGGER MODE Switch or EXTernal TRIGger Connector. The term General Purpose Interface Bus (GPIB) is used to describe the IEEE 488-1978 Standard. In addition, hexadecimal numbers will be enclosed by " " and decimals numbers by ' '.

2.1.1 POWER UP

For approximately two seconds after the power is applied to the Model 7085 all fifteen of the DELAY and WIDTH digits will display "8" and the two MEMory characters will continuously cycle. This allows the user to verify that all LED display digit segments are operational. During this time, the memory of the unit is being loaded with all zeros (Except for Option E - see Paragraph 2.5.2 below) assuring that whenever the power is turned off or interrupted for over several seconds, the units will have no output (zero delay and zero width). In addition, memory register "0" and memory bank "0" are selected. After any power interruption of several seconds duration, the contents of the memory will be lost (except for Option E - see Paragraph 2.5.2 below).

2.1.2 PERFORMANCE INFORMATION

(1) The circuitry of the Model 7085 synchronizes its internal clock with external or internal triggers to provide outputs devoid of the clock uncertainty normally found in counting circuits. In this manner, outputs are generated with extremely low jitter with respect to the input trigger. With the addition of Option B (See Paragraph 2.5.1 below), the internal clock reference of these units may be locked to an external standard at either 1 MHz or 10 MHz to obtain extremely stable and accurate delays and widths. Addition of Option E (See Paragraph 2.5.2 below) allows the unit to remember its settings when the power is off.

(2) Time measurements between signals (outputs and inputs) for the Model 7085 are made between the 50% points of the waveshapes. Rise and fall time measurements are made between the 10% and 90% points of each waveshape. Reference for all timing is directly at the respective connector on the front or rear panel. For these reasons care must be taken to match external cables if the accuaracy of the unit is to be maintained. (see Paragraph 2.1.4 below.)

2.1.3 OPERATING TEMPERATURE

(1) THE INTERNAL frequency reference of the Model 7085 is enclosed in a fast warm-up oven for stability. The units should be allowed to warm up for 10 - 15 minutes before high precision measurements are made. Less critical tests can be done immediately upon turn-on.

(2) The unit is provided with a fan for cooling. In the unlikely event that the fan is stopped and the ambient temperature is high, the unit will automatically shut down. Thus if the unit stops for no apparant reason, and the display is dark, check for excessively high ambient temperature and/or a blockage of the fan before taking other steps. The fuse should also be checked. If high ambient and/or fan blockage is discovered, reducing the temperature and/or unblocking the fan will automatically allow resumption of correct operation.

2.1.4 CABLES, ATTENUATORS AND OSCILLOSCOPES

The various outputs of the Model 7085 contain frequency components in excess of 100 MHz. All signal handling components such as loads, attenuators, cables, connectors and oscilloscopes should be able to pass these signals without distortion in order to maintain the inherent accuracy of the unit.

---------- NOTE ----------

Some sampling oscilloscopes have maximum input ratings that may be exceeded by the outputs of the Model 7085. When using such equipment be sure to turn down the AMPLITUDE Control or use an attenuator to lower the signal to a level acceptable to the oscilloscope.

As the reference points for calibration is directly at the input/output connectors, and at the 50% points of the waveshapes, the effect of cables in both distorting and delaying the signals is important. Such phenomena should always be considered when making critical timing measurements. For example, one foot of RG58/U cable has a delay of 1.5 ns. Therefore, if cables from the outputs are different in length by only 1.5 inches, the error induced will be greater than ±100 ps - the inherent accuracy of the unit. Also, should a mismatch occur in one of those cables, it is possible that reflections could occur at the 50% points of the waveshapes adding another cause of error.

2.2 OPERATING CONTROLS AND CONNECTORS

2.2.1 LINE VOLTAGE AND 115/230 SWITCH (rear panel)

The Model 7085 operates from either a 115-volt or a 230-volt, ±10%, 50/60 Hz line source. A slide switch on the rear panel selects of either of the line voltages. The switch is preset at the factory for the line voltage of the country to which the instrument is shipped. This switch should not be moved unless the line voltage is changed. Also note that when the switch is moved, the fuse should be changed to the proper value for the new line voltage. See Paragraph 2.2.2 below.

---------- WARNING ----------

IN THE EVENT THAT A TWO-WIRE ADAPTER OR OTHER CONNECTOR IS USED, CONNECT THE CHASSIS OR GREEEN WIRE TO A SUITABLE EARTH GROUND TO ELIMINATE SHOCK HAZZARD.

2.2.2 POWER SWITCH AND FUSE (rear panel)

All power is applied through the POWER ON toggle switch on the front panel. The DELAY/WIDTH Display will light when the unit is turned on. If the switch is in the ON position and the display is not lighted, either the fuse (rear panel) is blown or the unit is in an excess temperature condition owing to a fan blockage or an excessively high ambient temperature. Should the latter be the case, cooling the unit and/or removing the fan blockage will resume normal operation as soon as the internal temperature of the unit reaches a safe level. For 115 VAC operation the correct fuse value is 1.5 amp, Slo-Blo while for 230 VAC operation it is 0.75 amp, Slo-Blo.

2.2.3 EXTERNAL TRIGGER INPUT CONNECTOR

When the TRIGGER MODE SWITCH (Paragraph 2.2.6) is in the EXTernal TRIGger position, a signal of the proper levels will trigger the unit. The input impedance is 50 ohms. For proper triggering the input signal must be at least 200 mV peak-to-peak in amplitude, at least 10 ns in width and be 5 MHz or less in frequency. Peak inputs should not exceed +/- 15 volts and the average power of the input should not exceed 0.5 watts.

2.2.4 EXTERNAL TRIGGER SLOPE SWITCH

The SLOPE Switch determines whether the instrument will trigger on a positive-going or negative-going transition at the EXTernal TRIGger INPUT (Paragraph 2.2.3) connector. The trigger level is determined by the EXTernal TRIGger LEVEL Control (Paragraph 2.2.5).

2.2.5 EXTERNAL TRIGGER LEVEL CONTROL

The EXTernal TRIGger LEVEL Control determines the voltage level at which the Model 7085 will trigger. The LEVEL control varies the threshold from >+2 volts full clockwise to < - 2 volts fully counterclockwise. For a positive transition, triggering occurs when the input signal passes through threshold by at least 100 mV, and retriggering can occur after the input signal has dropped at least 100 mV below threshold. For a negative transition, the concept is identical but the directions are reversed.

2.2.6 TRIGGER MODE SWITCH AND FINE CONTROL

The TRIGGER MODE Switch selects the operating mode -- manual trigger, external trigger or internal trigger. In the MANUAL position, each time the MANUAL Button (Paragraph 2.2.7) is pressed a single cycle is produced. In the EXTernal TRIGger position, the EXTernal TRIGger INPUT Connector (Paragraph 2.2.3) is enabled and signals of the proper levels will operate the unit.

In the remaining positions, an internal repetition rate generator is used to trigger the unit. Six switch position select overlapping decade frequency ranges from 0.5 Hz to 5 MHz. The FINE Control adjusts the frequency over a 10:1 swing within each range.

2.2.7 MANUAL TRIGGER PUSHBUTTON

When the TRIGGER MODE Switch (Paragraph 2.2.6) is in the MANUAL position, the MANUAL Trigger Pushbutton generates one delay/width cycle each time it is depressed. If the button is pressed during a timing cycle, there is as remote chance that an erroneous width could occur. Therefore this should be avoided if possible.

2.2.8 ERROR LIGHT

Whenever the period of the trigger signal (either from the internal repetition rate generator or from an external trigger) is shorter than the delay time + the width time +160 ns, the error light will come on and stay on as long as the short period condition persists. The light being on indicates that the output from the unit may not be what is shown by the DELAY and WIDTH Display. If an error occurs only once, the light will remain on approximately 100 ms. The light can also come on

periodically during remote or front panel programming if a trigger occurs during the transfer of data from the Display or the programming controller to the internal counters of the unit.

One of the rockers on the rear panel ADRS/MODE Switch (Paragraph 2.2.24) determines whether or not a TTL level signal is presented to the GPIB bus when the light is on. Since this output is on the SRQ line and the unit is not capable of responding to a poll, the output is not strictly according to the IEEE 488-1978 Standard. The user is therefore cautioned to use the ERROR output selection of the ADRS/MODE switch with caution. See Subsection 2.4 for more details.

If the External Reference, Option B, is present, the ERROR Light will come on whenever a signal is present at the EXTernal REFerence INPUT Connector (rear panel) and the unit is not locked to it. This could occur either if the EXTernal REFerence Switch is in the wrong position or if the external signal deviates from the correct frequency by more than $\pm 1 \times 10^{-5}$. See Paragraph 2.5.1 for more details.

2.2.9 INITIAL OUTPUT CONNECTOR

The initial pulse occurs at the beginning of each delay/width cycle. When zero delay is set in the DELAY Display the leading edge of this pulse occurs at the same time as the start of the NORMal, COMPlement and NEG/ECL OUTPUTs. The pulse is > +5 volts in amplitude into a 50-ohm load from a low impedance source. The width is nominally 15 ns.

Note that the best waveshapes are obtained when this output is terminated in 50 ohms. If a higher impedance is to be used, better results are obtained if a parallel resistance is used at the load to simulate 50 ohms. Similarly, a series resistance should be used if the load is less than 50 ohms.

2.2.10 NORMAL AND COMPLEMENT OUTPUT CONNECTORS

The output from the NORMal Connector is a pulse which starts after the time set in the DELAY Display and has the width set in the WIDTH Display. The pulse is positive during the width time. It is adjustable in amplitude from < +0.5 volts to > +5.0 volts by the NORMal AMPLITUDE control.

The output from the COMPlement OUTPUT connector is the complement of the NORMal OUTPUT. That is when the NORMal output is positive, the COMPlement output is low (near ground). The timing of the pulses is identical. It is adjustable in amplitude from < +0.5 volts to > +5.0 volts by the COMPlement AMPLITUDE control.

Note that the best waveshapes are obtained when this output is terminated in 50 ohms. If a higher impedance is to be used, better results are obtained if a parallel resistance is used at the load to simulate 50 ohms. Similarly, a series resistance should be used if the load is less than 50 ohms.

2.2.11 AMPLITUDE CONTROLS

The AMPLITUDE Controls are concentric knobs which independently set the NORMal and COMPlement output levels. They vary their respective outputs from < +0.5 volts to > +5.0 volts when the outputs are terminated in 50 ohms. The rear panel NEGative/ECL OUTPUT (Paragraph 2.2.21) is not affected by either of these controls.

2.2.12 EDIT PUSHBUTTONS

These fifteen buttons directly under the DELAY and WIDTH Displays are used to edit the setting in the display. Pushing one of these buttons causes the corresponding LED display digit to blink indicating this is the decade that can be preset and that the instrument is in the Edit Mode. NOTE: whenever a digit is blinking (i.e. in the Edit Mode), the display is no longer guaranteed to indicate the actual instrument output. The Edit Mode allows the data in the Display to be altered without changing the instrument output. Pushing a black Data button, 0 through 9 (Paragraph 2.2.15) will enter the appropriate value and then cause the next digit on the right to blink. The user may then continue to enter numbers sequentially, skip to another decade by pressing another EDIT button or cease editing. Pushing the UPDATE Button (Paragraph 2.2.16) takes the instrument out of the Edit Mode and lights the LED alongside the button. The Display will then show the actual output of the instrument.

The EDIT Pushbuttons are grouped eight for delay and seven for width. The nomenclature over each button corresponds to the weight of that digit. For example, the 10 over the left most button means that an "8" in the corresponding display digit would have the value of 80 ms because it is the "ms" grouping and lined up with the number "10".

2.2.13 DELAY AND WIDTH DISPLAY

The Display shows the delay and width output of the unit only when the LED next to the UPDATE Pushbutton is lit (Paragraph 2.2.16). At any other time it may or may not indicate the current instrument output. The UPDATE LED will be extinguished indicating the Edit Mode (Paragraph 2.2.12)is in effect by pushing any Control, Data, MEMory or EDIT button other than REMote ENable and SCAN (Paragraphs 2.2.19 and 2.2.20 respectively).

In the Edit Mode the user may alter the Display without affecting the output of the unit. The Edit Mode is terminated by pushing the UPDATE button. If in doubt as to the output of the instrument, and the display shows the desired values, pushing the UPDATE button will will cause the UPDATE LED to light and assure that the desired output is being produced.

In the Remote mode (the REMote LED is on), the Display will show the latest setting to be sent to the instrument over the GPIB (Subsection 2.4). However it may or may not show the actual output depending upon whether or not an update signal was transmitted.

2.2.14 MEMORY DISPLAY AND PUSHBUTTONS

The MEMory Display shows the user which of the four memory banks and sixteen registers (sixteen banks and sixteen registers with Option E) is being used. The banks and registers are numbered in HEX code "0" to "F". The MEMory buttons in conjunction with the Data Entry Buttons (Paragraph 2.2.15) select the memory location to be displayed and used.

To change the memory location in use, a BANK or REGister button is pushed. This will cause the corresponding display above the button to flash. The desired REGister or BANK is then selected by pushing any of the sixteen Data Entry Keys. The selected memory location will then appear in the MEM display and the data stored in that memory location will appear in the DELAY and WIDTH Display. At this point the UPDATE LED (Paragraph 2.2.16) will not be lit indicating that the displayed setting is not the current instrument output. Pushing the UPDATE button will light the LED and cause the timed output to be the same as the displayed setting.

If power is interrupted for more than a few seconds, all stored data will be lost and every memory location will contain all zeros. In addition, the bank and register display should show that the memory location has been reset to the "00" address (Except for Option E, see Paragraph 2.5.2).

2.2.15 DATA ENTRY KEYBOARD

These 16 keys located to the right of the display are used to manually enter Delay and Width settings and select the desired MEMory REGister and BANK in use (Paragraph 2.2.14). The ten black buttons, '0' through '9' form a decimal keyboard and are used in conjunction with the EDIT Pushbuttons (Paragraph 2.2.12) to enter Delays and Widths. Together, the black and the gray buttons, "0" through ""F", are a hexadecimal keyboard which is used to manually select the MEMory REGister and BANK in use.

2.2.16 UPDATE PUSHBUTTON AND LIGHT

The UPDATE Pushbutton serves the function of transferring the setting that is currently in the DELAY and WIDTH Display to become the output of the instrument. When the button is pressed, the UPDATE LED will light and stay on until any other front panel button except SCAN or REMote ENable is pushed. As long as the UPDATE Light is on the Display shows the actual output of the Model 7085. When the light is off, ie. the instrument is in the Edit Mode (Paragraph 2.2.12), changing the display will not affect the output of the unit.

If there is some doubt as to the actual output of the instrument, and the DELAY and WIDTH Display shows the desired setting, the user can always push the UPDATE Pushbutton which activates the UPDATE Light and assuring that the output is the same as the Display setting.

When the UPDATE Button is pushed during a delay/width cycle, the setting in the Display will be produced by the unit the next time it is triggered, internally or externally. If the button is pushed between delay/width cycles, the first trigger after will generate a cycle with the old setting. The second and subsequent triggers, internal or external, will produce outputs with the new settings. This phenomenon only becomes important at very low trigger rates. See Paragraph 2.3.3 for more details.

2.2.17 NEXT PUSHBUTTON

Pressing the NEXT Pushbutton causes the unit to increment the memory in use by one. For example if the memory being shown in the MEMory Display were hex "00", depressing the NEXT Pushbutton once would cause the MEMory Display to show "01" and the setting in memory "01" would appear in the DELAY and WIDTH Display. Continuing to press the button will continue to cycle through the memory locations. If the display shows "4F" ("FF" if Option E is present - see Paragraph 2.5.2), depressing the NEXT Pushbutton will cycle the unit back to memory location "00".

NOTE: **the displayed setting is <u>not</u> the output of the unit until the UPDATE Pushbutton is pressed and the UPDATE Light comes on** (Paragraph 2.2.16).

2.2.18 HOME PUSHBUTTON

The HOME Pushbutton allows the user to <u>view</u> the setting in the memory that was in use the last time the UPDATE Pushbutton was pressed - i.e. the "home" memory. The delay/width reading displayed <u>will not</u> be the instrument's actual output if the displayed setting has been edited since the UPDATE Pushbutton was depressed.

NOTE: Some caution must be used in applying this function for the reasons mentioned above.

The HOME button does not change the memory location generating the instrument's outputs, but it does allow the user to look at the "home" memory so long as the HOME Pushbutton is being depressed. After the HOME button is released, the DELAY, WIDTH and MEMory Displays will show the setting present and the memory in use before the button was pushed.

2.2.19 REMOTE ENABLE/LOCAL PUSHBUTTON AND LIGHT

This latching pushbutton determines whether the instrument is being controlled by the front panel keys or by remote control via the GPIB (Subsection 2.4). As long as this button is in the LOCal position (out), the unit is in the local mode and the front panel keys will have control. When the button is latched in the REMote ENable position (in), the unit has been enabled for operation from the GPIB. NOTE: **the unit will remain in the local mode until it is addressed by a controller via the** GPIB. When that occurs, the REM ENable LED will come on and the front panel controls will be locked out. The unit will remain in the remote mode until the button is returned to the LOCal position or the power is turned off. The instrument cannot be returned by the IEEE Bus.

2.2.20 SCAN PUSHBUTTON AND LIGHT

When the SCAN Pushbutton is latched on (in) the SCAN LED will light and the Model 7085 will automatically sequence in ascending order through all its memory locations, one step each time the unit is triggered. This operation is analagous to the pressing of the NEXT Pushbutton (Paragraph 2.2.17) every time the unit is triggered when the SCAN Button is latched off (out).

This operating mode allows the user to enter up to 64 complete delay/width settings (256 with Option E) from the front panel or via the GPIB and then automatically sequence through them without GPIB control - one each time the unit is triggered. Thus, the 7085 can be used to sweep through a series of outputs automatically while altogether removed from a GPIB hookup. The scanning sequence can be started at any address in the memory by use of the BANK and REGister keys (Paragraph 2.2.14). When the unit reaches the 64th memory location (256th with Option E) it will recycle from the initially selected location.

Scanning can be aborted by interrupting the trigger pulses or unlatching the SCAN Button. The instrument is not internally designed to shorten the cycling of the memory through less than 64 (or 256 if Option E is present) steps. If, however, a shorter group of delay/width outputs is a sub-multiple of 64 (or 256 with Option E), two or more groups can be fitted into the memory so that no extraneous '0' outputs are produced when the unit is triggered through the upper memory locations.

Note that the maximum trigger frequency allowable in the Scan Mode is 10 KHz. This is necessary to permit the unit to transfer each new setting from the memory to the counters. Should this rate be exceeded, the ERROR Light may come on and the Display may blank itself or give an erroneous reading. Releasing the SCAN Pushbutton or reducing the input trigger rate will automatically return the instrument to normal operation.

2.2.21 NEGATIVE OUTPUT CONNECTOR (Rear Panel)

This output occurs coincident with and has the same width as the front panel NORMal and COMPlement outputs (Paragraph 2.2.10). The pulses are -1 volt into 50 ohms (-2 volts from a 50 ohm source) when the ECL/NORM Switch on the rear panel is in the NORMal position. When the switch is in the ECL position, and the signal is terminated into 50 ohms, the output from this connector is an ECL level pulse.

Note: if a 50-ohm termination is not used when the ECL mode is selected, the output levels will be more negative than normal and will not properly drive any ECL devices.

2.2.22 ECL/NORM SWITCH (Rear Panel)

This switch selects whether the NEGative OUTPUT Connector (Paragraph 2.2.21) produces pulses with a zero volt baseline (NORMal position) or pulses with ECL levels (ECL position). In the ECL position the NEGative OUTPUT must be terminated into 50 ohms or the levels will be too negative to properly drive any ECL device.

2.2.23 PROGRAM IN CONNECTOR (Rear Panel)

This connector conforms to the IEEE 488-1978 General Purpose Interface Bus (GPIB) Standard using metric hardware. The 24-pin connector is the input through which a suitable controller programs the functions of the Model 7085. The cable used for interconnection of the GPIB is not trivial and must conform to the IEEE standard. See Subsection 2.4 for further details.

2.2.24 ADRS/RESET MODE/ERROR OUT SWITCHES (Rear Panel)

The left five positions of this eight-position switch, marked 5...1, are used to set the instrument address. Any setting of address from "0" to "30" is allowable. The RESET MODE A is used to select whether or not the unit resets after a remote program update command. The RESET MODE B Switch has no affect in the Model 7085. The ERROR OUT switch determines whether or not the unit puts an output on the GPIB SRQ line when the front panel ERROR Light is on. Subsection 2.4 contains further details.

NOTE: **this function does not strictly adhere to the IEEE 488-1978 Standard because the Model 7085 is not capable of responding to a poll.**

Therefore it is advisable to use this function with caution. It is provided to assist the user in debugging a system or whenever the inability to determine which device is causing an interrupt is not a problem.

2.2.25 EXTERNAL CLOCK CONNECTOR (Option B) (Rear Panel)

When Option B is installed in the Model 7085, this connector is the input for the external clock signal. If there is no signal at this connector the Model 7085 will automatically be using its internal crystal oscillator as a reference. When a signal is connected to the EXTernal CLOCK Connector, the unit will lock on and use it as a reference unless it deviates from the frequency selected by the rear panel 1 MHz - 10 MHz Switch (Paragraph 2.2.26) by more than $\pm 1 \times 10^{-5}$.

If the external clock signal is too far off frequency, or if the wrong reference frequency is selected, the front panel ERROR light will come on and the instrument will have timing errors of approximately $\pm 1 \times 10^{-5}$. Setting the input frequency or rear panel switch correctly will reestablish proper operation. See Paragraph 2.5.1 for a more detailed explanation.

The error described above produces an error signal on the GPIB if the unit is in remote program mode and the rear panel ERROR OUT Switch is on. See Paragraph 2.2.24 and Subsection 2.4 for further details.

2.2.26 EXTERNAL CLOCK 1 MHz - 10 MHz SWITCH (Option B) (Rear Panel)

When Option B is installed in the Model 7085, this switch determines whether a 1 MHz or 10 MHz input to the EXTernal CLOCK Connector (Paragraph 2.2.25) will be used as the reference frequency. If the switch is in the wrong position, i.e. the input to the EXTernal CLOCK Connector does not correspond to in switch setting, the front panel ERROR Light will come on. See Paragraph 2.5.1 for a more detailed explanation.

2.2.27 INITIALIZE - STORE SWITCH (Option E) (Rear Panel)

When the extended memory with battery backup (Option E) is installed in the Model 7085, turning off power does not destroy the contents of the memory. Therefore, the user may not want to load '0' into all memory locations as is done in the Model 7085 without this option (Paragraph 2.1.1). This switch gives the user the option of disabling the '0' load function.

If the switch is in the INITialize position when power is turned on, the memory will be loaded with '0' in all locations as for the standard Model 7085. This is useful when the unit is first turned on or when totally new settings are desired. In the STORE position, the data in the memory is kept intact whether or not power is interrupted and the '0' load function is disabled. See Paragraph 2.5.2 for a more detailed explanation.

2.3 OPERATING INSTRUCTIONS

2.3.1 GENERAL

The Model 7085 Delay/Width Generator is a versatile general purpose instrument capable of generating very precise delays and widths. The following paragraphs will provide the user with a general set of guidelines for maximizing the usefulness of the instrument.

2.3.2 TURN-ON

Measurements with accuracies better than 10 ppm, require that the Model 7085 be allowed to warm up for at least 15 minutes. If accuracies on the order of 0.01% are satisfactory, the unit can be used immediately after turn-on.

For the first two to three seconds after the power switch is turned on (or after the power is interrrupted for several seconds), the DELAY and WIDTH Display digits will show '8' to verify that all LED segments are working. Simultaneously the MEMory Display digits will be cycled through their entire range. This occurs rapidly enough so that all segments can be checked. After this period, the DELAY and WIDTH Display will show all zeros, and the MEMory display will show "00" indicating that memory location hex "00" is being used.

During the time the MEMory Display digits are being cycled through their range, each memory location is being cleared of the random turn-on states by being loaded with all zeros. This provides the user with a known state - zero delay and width - from which to start programming the unit. If Option E is installed, the user has the option of enabling this function or not using the rear panel INITialize/STORE Switch (Paragraph 2.2.27). Paragraph 2.5.2 covers Option E in detail.

2.3.3 TIMING GENERATION

When the Model 7085 is first turned on, no output will occur from any connector. This is because all memory locations have been loaded with zero settings as describe in Paragraph 2.3.2. To obtain an output, data must be entered either through the front panel controls or via the GPIB and a suitable controller. The latter case is covered in Subsection 2.4. If Option E is installed, the unit may have outputs directly after turn-on depending upon the turn-on mode selected by the user. Paragraph 2.5.2 has more details.

To enter data from the front panel, the REMote ENable Pushbutton must be out (i.e. the unit is in the local mode). Any EDIT Pushbutton may be pressed to select the starting point of data entry. The digit above the button will begin to blink indicating that it is the one to receive data. Data keyboard Buttons, '0' to '9', may then be pushed sequentially until the desired delay/width settings are obtained. As the buttons are pushed, the blinking will move to the right indicating that the next data keyboard entry will go into that decade position. If the user starts in the DELAY section, data entry may continue into the WIDTH section without pushing another EDIT Pushbutton.

Alternatively, if only a few digits are to be entered or changed, the EDIT Pushbutton may be pushed for each decade and only one data keyboard button pushed each time. In either case, when the display setting is as desired the user has the option of pressing the UPDATE button causing the unit to generate the displayed setting or futher settings can be entered into other memory locations. Memory manipulation is discussed in Paragraph 2.3.4 and examples are given in Paragraph 2.3.5.

When the UPDATE Button is pushed during a delay/width cycle, the information in the Display is transferred into the the units internal counters at the end of the cycle. As a result, the next internal or external trigger to the unit will produce an output with the new data. However, should the UPDATE Button be pushed between cycles, as might occur at very low repetition rates, the data in the Display will not be loaded into the counters until the end of the next delay/width cycle. This means that the first trigger after the update will cause a cycle with the setting being produced prior to the update. The second and subsequent triggers will generate outputs with the updated setting.

2.3.4 MEMORY MANIPULATION

When power is first turned on, memory location hex "00" is in use and a "00" reading is shown in the MEMory Display. If only one setting is needed, this location will probably be adequate. However, if entries are to be made into any of the 63 other memory locations (255 with Option E), the procedure given in the following paragraphs may be used.

The MEMory Display consists of a two-digit hex number which is the address of a memory location that contains one complete instrument setting. The least significant digit is referred to as a REGister while the most significant digit is called a BANK. A BANK can be considered to have sixteen registers, and each register to hold one complete instrument delay/width setting.

To call up or enter data into any memory location the buttons under the REGister and BANK Digits are pushed followed by pushing the Data Key corresponding to the desired REGister or BANK. Either BANK or REGister may be pushed first, but a Data Key must be pushed between, or only one digit will change. It is also possible to change only the REGister or BANK.

For example if it is desired to call up memory location "E2", the BANK Pushbutton is pressed causing the BANK digit to blink. The "E" Data Key is then pushed entering that value into the display. The digit will cease blinking at this stage and it is possible to stop if desired. To complete the operation, the Register Pushbutton is pushed causing the REGister digit to blink. The "2" Data Key button is then pushed entering that value into the REGister display. The MEMory Display will now show "E2" and the data stored will be shown by the DELAY and WIDTH Display.

Once the desired memory has been called up, the user may immediately cause the unit to be ready to generate the stored delay/width setting by pushing the UPDATE Pushbutton. The outputs will then be producing the delay and width displayed when the instrument is triggered. Alternatively, new data could be entered into the location using the procedure described in Paragraph 2.3.3. If desired all 64 (or 256 for Option E) memory locations can be loaded with data in this manner.

2.3.5 EXAMPLES

Some examples of data entry procedures and memory manipulation may prove instructive to the user:

(a) The unit has just been turned on and it is desired to enter a delay of 100 ns and a width of 3.45 μs. The memory location is not important. One way to accomplish this is to first push the EDIT button below the '100' in the ns portion of the DELAY section of the front panel. The display digit above will flash. The '1' button is then pushed in the data keyboard. A 1 will appear in the decade selected, and the next digit to the right will flash. The DELAY Display will then read 00000100, the desired setting. Since no further delay digits need to be changed, the EDIT Button under the '1' in the Width μs section is pushed. Again the digit above will start blinking. The Data Key '3' is pushed causing a 3 to appear and the next digit to the right to blink. A '4' is then pushed followed by a '5'. The result will be a display in the WIDTH Display section of 0003450 indicating a width of 3.45 μs. To cause the displayed setting to become the output of the unit, the UPDATE Button is pushed. Blinking will stop and the UPDATE Light will come on to indicate that the setting being displayed corresponds to the output of the unit.

(b) To change the delay in example (a) to 110 ns leaving everything else the same, the EDIT Button under the '10' in the ns DELAY section is pushed. The digit above will blink. The '1' button in the data keyboard is then pushed to enter a 1 into the blinking decade. After the UPDATE button is pushed the unit will be ready to generate a 110 ns delay with the previously set width.

(c) A completely new setting is to be stored for future use in MEMory location "2F". To call up the correct location, the BANK Button is pushed. The number or character directly above will blink. The "2" on the data keyboard is pushed entering that value into the BANK display which will then cease blinking. Next the REGister Button is pushed causing its number or character to blink. The "F" button is pushed entering that letter into the REGister Display. The DELAY and WIDTH Display will now show whatever was <u>previously</u> stored in memory location "2F".

If the desired new setting were 12.345678 ms delay and 1.234567 ms width, the entire entry could be made as follows: press the EDIT Button under the '10' in the ms portion of the DELAY section of the front panel. This will cause the left-most digit (msd) to blink. The Data Keyboard buttons '1', '2', '3', '4', '5', '6', '7', '8', '1', '2', '3', '4', '5', '6', '7' are then pushed in sequence. Each push of a data keyboard button enters the value of the key pushed into the flashing decade and causes the next digit to the right to flash. When the DELAY section of the Display is full, the procedure continues into the WIDTH section. When the above sequence is completed, the DELAY Display will show 12345678 and the WIDTH section 1234567 - the desired setting.

Since it is not desired to execute this setting immediately, the UPDATE button is not pushed. Other memory locations may be loaded in this manner or whatever else is to be done may continue.

2.3.6 MULTIPLE DELAYS AND WIDTHS

Because the Model 7085 exhibits very low jitter when triggered, multiple units may be used to generate parallel or sequential delays and widths with very low jitter between edges.

For parallel operation. all units are triggered from the same source. If identical cables are used, the outputs from all units will be very close for the same delay settings and the widths will be within the specified accuracy of each other. Depending upon the rise time of the triggering source, the delays can be matched by varying the TRIGGGER LEVEL front panel controls. This will cause the various units to trigger at different points on the input waveshape resulting in slightly different delays for each unit.

For serial operation, the first unit is triggered from an external source or internally, and the next unit is triggered from the NORMal, COMPlement or NEGative OUTPUT of the first. This procedure may continue for any number of units desired. The result will be a series of pulses with controllable delays and widths. Note that the insertion delay of each succeeding unit will be added to its delay setting.

2.4 REMOTE PROGRAMMING

2.4.1 GENERAL

The Model 7085 conforms to the IEEE 488-1978 Standard (GPIB) as applied to instruments which are listeners only. A complete description of this standard is beyond the scope of this manual. The reader is referred to the standard itself or the many publications available which describe its operation. This portion of the manual will present a brief look at the basics of the GPIB, programming instructions and other general operating instructions for using the BNC Model 7085 in a system using the IEEE standard. Hexadecimal numbers will be enclosed by " " and decimal numbers by ' '.

2.4.2 THE IEEE 488-1978 STANDARD (GPIB)

The IEEE 488-1978 Standard, commonly referred to as the General Purpose Interface Bus (GPIB), is a byte-serial, bit parallel interface system primarily defined for use with programmable instrument systems. The standard defines all circuits, cables, connectors and control protocol for unambiguous data transfer between devices.

The GPIB has the following defined operational constraints:

1. No more than 15 devices can be interconnected by a single contiguous bus.
2. Total transmission length is limited to 20 meters, or 2 meters times the number of devices, whichever is less.
3. Data rate through any signal line must be less than or equal to 1 megabit/second.
4. All data exchange is digital.

The system is constructed with 16 transmission lines - 8 data bus lines for transmitting ASCII characters. 3 byte transfer control lines (handshake), and 5 general interface management signal lines. These sixteen lines may employ either open-collector (modified by the termination networks on the bus) or three-state driver elements with certain constraints. A true or "1" state is indicated by a low voltage level (i.e. less than +0.4 volts) and the "0" or false state is indicated by a high voltage (over +2.4 volts) as determined by the bus terminating networks.

Figure 2.1 gives a brief description of the GPIB Configuration and operation. The following is a description of the sixteen bus lines incorporated in the GPIB:

THE IEEE-488 BUS

The IEEE Interface Bus transfers data and commands between the components of an instrumentation system on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel to the signal lines.

Eight of the lines (DIO1-DIO8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and messsage transfer is asynchronous, coordinated by the three handshake lines (DAV, NRFD, NDAC). The other five lines are for control of bus activity.

Devices connected to the bus may be talkers, listeners, or controllers. The controller dictates the role of each of the other devices by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (DIO1-DIO8). Addresses are set into each device at the time of system configuration either by switches built into the device or by jumpers on a PC board. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers will be automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of the five control lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using the ASCII code. When ATN is false, any code of 8 bits or less understood by both talker and listener(s) may be used.

The other control lines are IFC, REN, SRQ, EOI.

IFC (interface clear) places the interface system in a known quiescent state.

REN (remote enable) is used with other coded messages to select either local or remote control of each device.

Any active device can set the SRQ (service request) line true. This indicates to the controller that some device on the bus wants attention, say a counter that has just completed a time-interval measurement and wants to transmit the reading to a printer.

EOI (end or identify) is used by a device to indicate the end of a multiple-byte transfer sequence. When a controller sets both ATN and EOI lines true, each device capable of a parallel pole indicates its current status on the DIO line assigned to it.

In the interest of cost-effectiveness it is not necessary for every device to be capable of responding to all the lines. Each can be designed to respond only to those lines that are pertinent to its function on the bus.

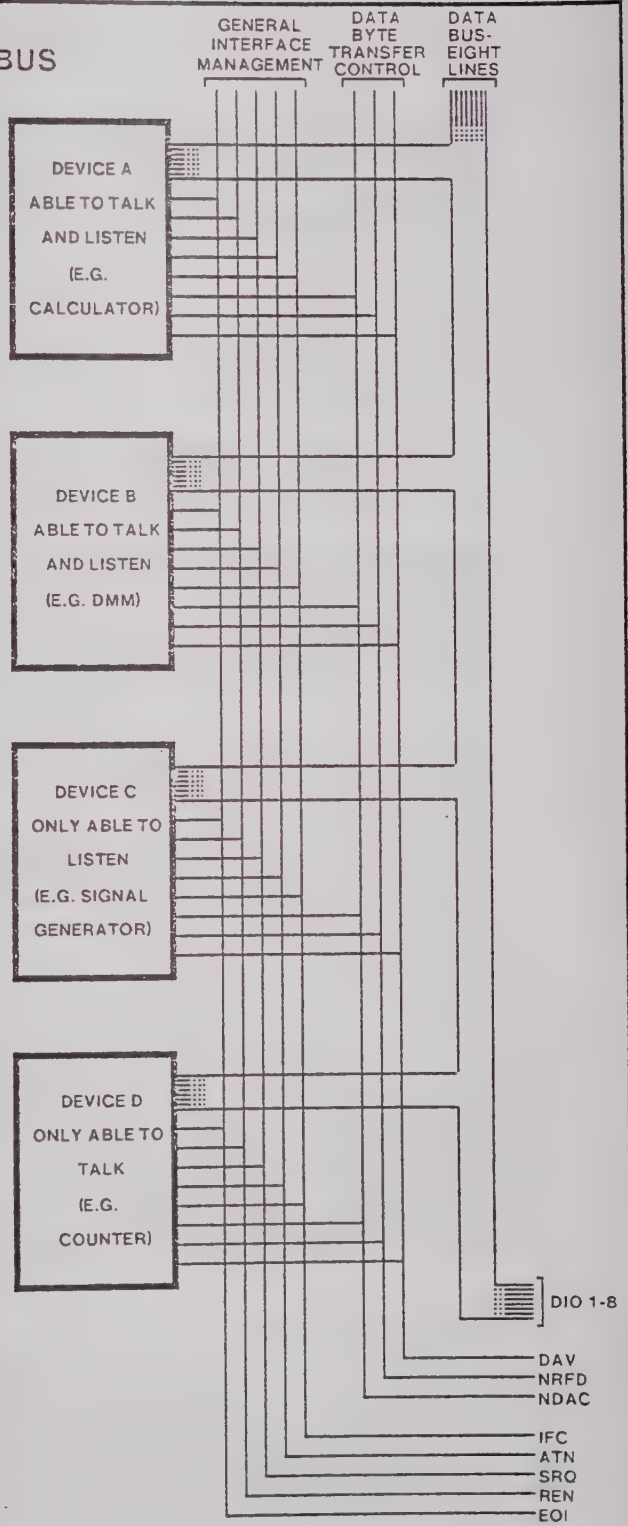


FIGURE 2.1

DIO-1 -- DIO-8 (Data Input/Output) --- These are data carrying message lines. They carry either data or address information depending on the condition of the ATN line.

DAV (Data Valid) --- One of the three handshake lines used to indicate availability and validity of information on the DIO lines. DAV indicates that data is on the DIO lines.

NRFD (Not Ready for Data) --- Handshake line that indicates that all devices are or are not ready for data.

NDAC (Not Data Accepted) --- Handshake line used to indicate the acceptance of data by all devices.

ATN (Attention) --- Bus management line used to specify how data line information is to be interpreted and which devices must respond. When ATN is true, the DIO lines carry addresses or commands. When false they carry data.

IFC (Interface Clear) --- Bus management line used to place the system in a known quiescent state. Puts talkers and listeners in their idle states.

SRQ (Service Request) --- Bus management line used by a device to indicate a need for service and to request an interrupt. The Model 7085 does not use this line in the normal manner because it cannot respond to a poll.

REN (Remote Enable) --- Bus management line which helps select between two alternate sources of programming data, i.e. front panel controls and GPIB. The model 7085 does not respond to this line.

EOI (End or Identify) --- Bus management line used to indicate the end of multiple byte transfers or with ATN to perform a parallel polling sequence. The Model 7085 does not respond to this line.

2.4.3 SYSTEM CONNECTION

Because of the bit-parallel, byte-serial nature of the GPIB, the Model 7085 is programmed by a series of ASCII characters as supplied by a suitable bus controller. The mechanics of addressing, handshaking and data transfer is provided by the combination of the controller and the Model 7085, so to program the unit it is only necessary to connect a controller to the unit via a suitable cable (such as an Amphenol Interface Bus Cable Assembly number 408-30111-302), select the proper device address (rear panel switches) and make sure the front panel REMote ENable/LOCal Pushbutton is in the REM EN position (in). It should be noted that the specifications of the interconnecting cables are not trivial and must be met in order to strictly conform to the IEEE standard. Metric hardware must be used on the cable.

2.4.4 PROGRAMMING DATA

The Model 7085 programming field consists of a maximum of nineteen ASCII characters: two select the memory location to be used; fifteen are the delay and width data; one is an address character indicating the starting point of the new data; and one is a character indicating it is desired to update the unit. A total of 64 memory registers are available (256 with Option E), each capable of storing one complete delay and width setting. In addition to delay and width entry, three extra functions are available via the GPIB: Reset, Next and Scan. The Reset function causes memory location "00"

to be used and is available only through the GPIB. The Next and Scan functions operate through remote programming in the same manner as for front panel control. See Paragraphs 2.2.18 and 2.2.20. Table 2.1 lists the characters and bit patterns for calling up the extra and normal functions. Figure 2.2 shows the programming field for the Model 7085 with an example message.

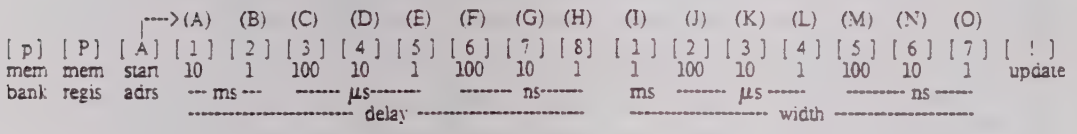

(A) (B) (C) (D) (E) (F) (G) (H) (I) (J) (K) (L) (M) (N) (O)
[p] [P] [A] [1] [2] [3] [4] [5] [6] [7] [8] [1] [2] [3] [4] [5] [6] [7] [!]
mem bank
mem regis
start adrs
10 1 100 10 1 100 10 1 1 100 10 1 100 10 1
update
--- ms ---
------ µs------
-------- ns------
ms -------- µs ------
---------- ns -----
delay
width

Figure 2.2: Programming field for the Model 7085

The example message of Figure 2.2 contains the maximum number of characters: three alpha characters followed by fifteen data digits followed by a character which tells the instrument to execute the commands given in the preceding message. The command shown is similar to example (c) in Paragraph 2.3.5 - it will enter a setting of 12.345678 ms delay, 1.234567 ms width and cause the unit to update. In the following paragraphs any character or digit in brackets, [ ], is a GPIB command.

The alpha characters are names for a register, bank or start address. The significance of each of the characters along with its bit pattern is given in Table 2.1. From this table it can be seen that the characters in the Figure 2.2 programming field example have the following significance: the first, [p], causes a "0" bank location while the second, [P], causes a "0" register location. The third alpha character tells the instrument at what digit to start entering the subsequent data. In this case [A] indicates data is to start in the first (most significant) digit. The letters in parentheses in Figure 2.2 are the start addresses for the digits below. The fifteen numbers following the start address are the delay and width setting to be entered. The first [1] is in the 10 ms delay slot and will therefore load the value of 1 into that location. In a similar manner the remaining numbers load into their corresponding locations. The last character is an update command. When present, it tells the unit to start producing the preceding setting as soon as it is received. If it is not received, the setting will remain unused in the memory location designated until it is called up. Table 2.2 gives a complete list of characters that may be used as an update command.

If only a minor alterations are to be made, it is possible to start at the location of the first digit that is to be changed and send only the new values. In addition, if the memory location is not to be changed, the first two alpha characters are not needed. Continuing the above example will illustrate this. Transmitting the command [G 1 1 !] would first alter the 10 and 1 ns delay digits, causing both to be 1, and then would cause the unit to update. As a result, immediately upon receipt of the [!] update command the delay of the unit would change to 12.234511 ms and the width would remain unchanged.

Some further examples of typical GPIB messages will help the user understand the editing capabilities of the Model 7085 when used with the GPIB. A reminder that in this section " " encloses hexadecimal numbers and ' ' decimal numbers.

(1) It is desired to change all digits of delay and width, load the setting into memory location designated by hex "2B" and be ready to generate the new setting immediately. From Table 2.1 it is seen that bank "2" is addressed by [r] while register "b" is addressed by [[ ] (the middle bracket - [- is an ASCII command, not just the designation of a command).

(a)

START LOCATION	ASCII CHARACTER ADDRESS	BIT NUMBERS							
		B8	B7	B6	B5	B4	B3	B2	B1
DELAY 10 ms	A	X	1	0	0	0	0	0	1
DELAY 1 ms	B	X	1	0	0	0	0	1	0
DELAY 100 us	C	X	1	0	0	0	0	1	1
DELAY 10 us	D	X	1	0	0	0	1	0	0
DELAY 1 us	E	X	1	0	0	0	1	0	1
DELAY 100 ns	F	X	1	0	0	0	1	1	0
DELAY 10 ns	G	X	1	0	0	0	1	1	1
DELAY 1 ns	H	X	1	0	0	1	0	0	0
WIDTH 1 ms	I	X	1	0	0	1	0	0	1
WIDTH 100 us	J	X	1	0	0	1	0	1	0
WIDTH 10 us	K	X	1	0	0	1	0	1	1
WIDTH 1 us	L	X	1	0	0	1	1	0	0
WIDTH 100 ns	N	X	1	0	0	1	1	0	1
WIDTH 10 ns	N	X	1	0	0	1	1	1	0
WIDTH 1 ns	O	X	1	0	0	1	1	1	1

(b)

	0		1	1	BIT NUMBERS						
	1		1	0							
	1		1	1							
SPECIAL FUNCTION		BANK/ REGISTER NUMBER	ASCII CHAR ADDR		B7	B6	B5	B4	B3	B2	B1
NAME	ASCII		BANK	REGISTER	↓	↓	↓	↓	↓	↓	↓
RESET	`	0	p	P				0	0	0	0
NEXT	a	1	q	Q				0	0	0	1
SCAN ON	b	2	r	R				0	0	1	0
SCAN OFF	c	3	s	S				0	0	1	1
		4	t	T				0	1	0	0
		5	u	U				0	1	0	1
		6	v	V				0	1	1	0
		7	w	W				0	1	1	1
		8	x	X				1	0	0	0
		9	y	Y				1	0	0	1
		A	z	Z				1	0	1	0
		b	{	[				1	0	1	1
		C	|	\				1	1	0	0
		d	}	]				1	1	0	1
		E	~	^				1	1	1	0
		F	DEL	_				1	1	1	1

TABLE 2.1: Bit patterns for the various instructions in the Model 7085. (a) start location addresses. X = do not care. (b) memory and special character addresses.

ASCII CHARACTER	BIT NUMBERS							
	B8	B7	B6	B5	B4	B3	B2	B1
SP	X	0	1	0	0	0	0	0
!	X	0	1	0	0	0	0	1
"	X	0	1	0	0	0	1	0
#	X	0	1	0	0	0	1	1
$	X	0	1	0	0	1	0	0
%	X	0	1	0	0	1	0	1
&	X	0	1	0	0	1	1	0
'	X	0	1	0	0	1	1	1
(	X	0	1	0	1	0	0	0
)	X	0	1	0	1	0	0	1
*	X	0	1	0	1	0	1	0
+	X	0	1	0	1	0	1	1
,	X	0	1	0	1	1	0	0
-	X	0	1	0	1	1	0	1
.	X	0	1	0	1	1	1	0
/	X	0	1	0	1	1	1	1

TABLE 2.2: Characters and bit patterns allowable for update command. Recommended character for use is [!]. X = do not care condition.

Data must be entered starting at the most significant digit, therefore [A] is the start address required. Assume the desired setting is 87.654321 ms delay and 7.654321 ms width. The last character was selected from among those listed in Table 2.2 as allowable UPDATE commands. Using this information, the total message can be constructed to be:

[r [A 8 7 6 5 4 3 2 1 7 6 5 4 3 2 1 !]

(2) The 1 μs digit of delay in Example (1) is to be changed to '8' without changing memory location or any other part of the setting. Three characters need be sent by the controller: [E 8 !]. The [E] is the start address for the 1 μs delay slot (Table 2.1), the [8] is the value to be entered in that decade, and the [!] is the update command (Table 2.2).

(3) Memory location "00" is to be preloaded with a setting (111 ns delay and 222 ns width) which is not be generated by the Model 7085 immediately. From Table 2.1, it is seen that bank "0" is designated by [p], register "0" by [P], the 100 ns delay starting location by [F] and the 100 ns width location by [M]. The command that must be sent to the unit is: [p P F 1 1 1 M 2 2 2]. Note that no update character is sent after the delay and width data field. This means the unit will not generate this setting upon being triggered, but merely store it in memory location "00".

(4) The setting stored in Example (3) must now be executed. Assuming that the unit is not already using the desired memory location, three characters need be sent - the register, bank and an update command: [p P !]. As soon as the [!] command is received, the unit will set up to generate the setting stored in memory location "00" as called out by [p P].

(5) When digits must be changed in various locations in the programming field it is not necessary to send a maximum message. For example, if directly after turn-on, (the unit will contain zero delay and width and be using memory location "00" unless Option E is present) it is desired to set up 1 μs delay and 200 μs width using the same memory location, the minimum command would be: [E 1 J 2 !]. The [E] addresses the 1 μs digit, the [1] enters '1' into it, the [J] addresses the 100 μs width digit, the [2] enters '2' into it and the [!] causes the instrument to be updated. This means the unit will be ready to generate the new setting as soon [!] is received.

(6) It is desired to go directly from another memory location to "00" using the reset command. When the [\ ] command (see Table 2.1) is received the unit will immediately be in the Edit mode at memory location "00". A new setting can be entered if required. To generate the setting stored in memory location "00", the command would be [\ !].

(7) The unit is currently using memory location "10" and it is desired to generate the setting stored in memory location "11". This can be done using a single character command using the Next function. When the unit receives [a !] (see Table 2.1), as soon as it is triggered, it will produce the outputs corresponding to the setting stored in the memory location with the next higher number than the one being used - in this case - "11".

(8) Sixty-four settings have been loaded into the unit's memory. It is desired to sequentially generate these settings - one each time the unit is triggered (either internally or externally). The Scan command is used for this purpose. When [b] (Table 2.1) is received, the unit will begin to sequentially generate the output settings stored in the memory. When the 64th memory location is reached, the unit will start over at the starting point.

(9) It is desired to stop the Scan function started in Example (8). This is accomplished by sending the command [c] (Table 2.1). This will immediately turn off the Scan mode and return the unit to nomal operation.

2.4.5 OPERATING CONSIDERATIONS

The Model 7085 conforms to a subset of the GPIB standard. Within this subset, the EOI and REN functions are not implemented and are therefore ignored. In addition, data on line DIO8 is ignored.

Other operational features that should be noted are:

(1) If the REM EN/LOC Pushbutton is in the REM EN position, the unit will automatically power up in the LOCal mode. It will remain in the is mode until the unit is addressed by a controller on the GPIB. It will then switch to remote mode and remain in that mode until the unit is manually switched to LOC or until the power is switched off.

(2) On power up, the unit will automatically have memory location "00" in use. If this is satisfactory, the first two characters in the programming field need not be used. For Option E, the unit will come up in the last memory location selected before the unit was turned off (or power was interrupted) provided the INIT/STORE Switch (rear panel) is in the STORE position. If the INIT/STORE Switch is in the INITialize, position the unit will come up with all zeros just as a Model 7085 without Option E.

(3) The Model 7085 accepts all listener addresses except 31. The address is set by means of the 5 rear panel ADRS Switches. The ASCII code corresponding to the address switch settings is shown in Table 2.3. It should be noted that the ASCII characters listed are addresses only during ATN true.

(4) If the Model 7085 is triggered precisely during the time data transfer is occuring, i.e. during or for 10 μs after and update command, an erroneous output cycle may occur. However subsequent cycles will be correct. If it is necessary to assure that no wrong outputs are produced, the unit must not be triggered during, or for 10 μs after the transmission of an update character on the DIO bus.

To reduce this effect, RESET MODE A switch is provided on the rear panel. When this switch is in the ON position, the unit is reset during the data transfer period. In this context, reset means the unit will abort any delay/width cycle in process and the new setting will be jammed into the internal counters. This function does not completely eliminate erroneous outputs but reduces them to cases where the trigger occurs very close to the beginning or end of the data transfer process. RESET MODE B Switch has no affect in the Model 7085.

(5) When the update command , [!], is received <u>during</u> a delay/width cycle, the new data is loaded into the internal counters of the unit at the end of the cycle. The next trigger, internal or external, will generate an output with the new setting. However, when the update occurs <u>between</u> delay/width cycles, the information is not transferred until the end of the next cycle. This means that the first trigger, internal or external, after the update will generate an output with the old setting. The second and subsequent triggers will produce delay/width cycles with the new setting.

If it is not acceptable to have the first output delay/width cycle after an update command occur with the old setting, the RESET MODE A Switch (rear panel) may be used. When this switch is in the ON position, immediately upon receiving the update command, the unit will abort the cycle that is in process and load the new data into the counters. The next trigger, internal or external will then have the new setting.

ASCII CHARACTER	BIT NUMBERS							
	B8	B7	B6	B5	B4	B3	B2	B1
SP	X	0	1	0	0	0	0	0
!	X	0	1	0	0	0	0	1
"	X	0	1	0	0	0	1	0
#	X	0	1	0	0	0	1	1
$	X	0	1	0	0	1	0	0
%	X	0	1	0	0	1	0	1
&	X	0	1	0	0	1	1	0
'	X	0	1	0	0	1	1	1
(	X	0	1	0	1	0	0	0
)	X	0	1	0	1	0	0	1
*	X	0	1	0	1	0	1	0
+	X	0	1	0	1	0	1	1
,	X	0	1	0	1	1	0	0
-	X	0	1	0	1	1	0	1
.	X	0	1	0	1	1	1	0
/	X	0	1	0	1	1	1	1
0	X	0	1	1	0	0	0	0
1	X	0	1	1	0	0	0	1
2	X	0	1	1	0	0	1	0
3	X	0	1	1	0	0	1	1
4	X	0	1	1	0	1	0	0
5	X	0	1	1	0	1	0	1
6	X	0	1	1	0	1	1	0
7	X	0	1	1	0	1	1	1
8	X	0	1	1	1	0	0	0
9	X	0	1	1	1	0	0	1
:	X	0	1	1	1	0	1	0
;	X	0	1	1	1	0	1	1
<	X	0	1	1	1	1	0	0
=	X	0	1	1	1	1	0	1
>	X	0	1	1	1	1	1	0

TABLE 2.3 Acceptable listen addresses. Note that these addresses are valid only when ATN is true.

2.4.6 PROGRAMMING CONNECTOR

The programming connector on the rear panel conforms to the IEEE 488-1978 Standard (GPIB) and uses metric hardware. The user should make sure that the cable assembly used is metric. (The Amphenol 408-30111-302 assemblies are adequate.) Metric threads on a GPIB cable are easily recognized as the standard requires that metric GPIB cable assemblies have black hardware. Table 2.4 gives the pin assignments for the programming connector.

2.5 OPTIONS

2.5.1 EXTERNAL FREQUENCY REFERENCE - OPTION B

Option B provides the user with the capability of phase locking the internal frequency reference system of the Model 7085 to an external frequency standard that is within $\pm 1 \times 10^{-5}$ of 1 MHz or 10 MHz. This allows the generation of long time delays and widths with accuracies mainly limited by the precision of the external frequency standard used.

The EXT CLOCK connector on the rear panel is the input for the external frequency standard. The frequency to be used is selected by the 1 MHz - 10 MHz slide switch on the rear panel. The signal must have TTL compatible levels and a minimum pulse width of 40 ns.

With no signal at the EXT CLOCK connector, the Model 7085 uses its internal frequency reference system. When a proper frequency signal (selected by the 1 MHz-10 MHz Switch) is present, the unit uses the EXT CLOCK as reference. If the signal frequency is different from the 1 MHz-10 MHz Switch, or is off by more than $\pm 1 \times 10^{-5}$, the ERROR light will come on indicating something is wrong, and the unit will have timing errors approximately 1×10^{-5} in the opposite direction of the external clock signal error. This means that if the frequency is low - a minus error, the period will be too long. If the frequency is high - a plus error, the period will be too short. Setting the input frequency or rear panel switch correctly will bring the unit back to proper operation.

The error signal produced when the EXT CLOCK input signal frequency is incorrect will appear on the GPIB SRQ line if the ERROR OUT Switch (rear panel) is in the ON position and the unit is in the remote mode. Since the Model 7085 cannot respond to a poll, this function should be used with caution. See Subsection 2.4 for further details.

2.5.2 OPTION E

Option E adds an expanded memory with battery backup to the standard Model 7085. It provides the user with 256 complete delay/width settings which can be retained for up to three weeks when the battery is properly charged. All other functions of the standard Model 7085 are retained.

When this option is installed, turning off the unit does not destroy the memory. Therefore the user may not desire to load '0' into all memory locations when the power is first turned on or when it is interrupted for several seconds. The INITialize/STORE Switch (rear panel) provides the option of selecting or turning off the '0' load at turn-on capability. When the Switch is in the INITialize position, the unit loads zeros into all memory locations when power is first turned on. Also, memory location "00" is selected and displayed in the MEMory Display.

When the switch is in the STORE position, the turn-on zero function is disabled, and the unit will retain the settings entered before the power was turned off or interrupted. When the power is returned, the unit may not come up with the delay/width setting it had when the power was turned off, but all data in the memory will have been retained (unless more than three weeks has elapsed).

CONTACT	SIGNAL LINE
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	SHIELD

CONTACT	SIGNAL LINE
13	DIO5
14	DIO6
15	DIO7
16	DIO8
17	REN
18	Gnd. (6)
19	Gnd. (7)
20	Gnd. (8)
21	Gnd. (9)
22	Gnd. (10)
23	Gnd. (11)
24	Gnd. Logic

TABLE 2.4: Programming connector pin assignments. Note: Gnd. (#) refers to signal ground return of referenced contact.

REVISIONS			
LTR	DATE	DESCRIPTION	BY

DATA ENTRY

EDIT KEYS (15)

TO DATA KEY EDIT KEY

EDIT KEY SIGNAL

EDIT WIDTH 1ms

EDIT DELAY 10ms

HEX SIGNAL

DBL. SIGNAL

DATA KEYS (16)

DATA ENTRY CIRCUITS & MEMORY CIRCUITS PCB 7085-2 (DWG. D-7085-31 & D-7085-32)

Z4 74LS154

OUTPUTS

E	WIDTH		10ms
D			100ms
C			1 MS
B			10MS
A			100µS
9			1ms
8	DELAY		10 ms
7			100 ms
6			1 MS
5			10 MS
4			100 µS
3			1ms
2			10ms

+5V, VCC, GND, SCAN CLK, DATA BUS, BANK BLNK, DISPLAY BUS, REGISTER BLINK

Z3 9368 — INPUTS A B C RE — SEGMENT OUTPUTS D e d c b a g f RBO — VCC GND EN

Z2 9368 — +5V, C .05, D C B A

R1: 7 x 270

DS16 HDSP-3533 — BANK — CATH

R2 7 x 270

DS17 HDSP-3533 — REGISTER — CATH.

Z5 74LS154 — DISPLAY BUS D C B A — VCC GND G1 G2

DATA DISPLAYS

Z13 75453	DS15 HDSP-3533	WIDTH
Z12 75453	DS14 HDSP-3533	10
Z1 75453	DS13 HDSP-3533	100
Z10B 75453	DS12 HDSP-3533	1MS
Z9 75453	DS11 HDSP-3533	10
Z8 75453	DS9 HDSP-3533	100
Z7 75453	DS8 HDSP-3533	1MS
Z6 75453	DS7 HDSP-3533	DELAY
	DS6 HDSP-3533	1MS
	DS5 HDSP-3533	10MS
	DS4 HDSP-3533	1S
	DS3 HDSP-3533	10S
	DS2 HDSP-3533	1MS
	CAT DS1 HDSP-3533 SEGMENT ANODE e d c b a g f	10MS

+5V, C2 .05

Z10A 75453 — 2A 2B 2Y — R3 470 — Q1 2N3646 — R4 470

R5 470, R6 470

+5V, SEGMENT OUTPUTS e d c b a g f — Z1 8881 — VCC GND TST E INPUTS D C B A

RAM BUS D0 D1 D2 D3 — DATA BUS — POWER ON GATE

DATA ENTRY & MEMORY CIRCUITS PCB 7085-2 (DWG. D-7085-31 & D-7085-32)

+5V, DS18 SCAN, R105 470, OFF, ON, 33µF 25V, Z14 74S14

BANK, REGISTER, REMOTE, HOME, UPDATE, NEXT, LCL, EN — S35, S34, S33, S32, S31, S30, S36

Z14 74S14, Z14 74LS14

DS19 UPDATE, R7 470

DS20, R8 470, R9 22K

DS10, R9 470

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. 7416 PIN 7 IS GND, PIN 14 IS VCC.
2. 75453 PIN 4 IS GND PIN 8 IS VCC.
3. ALL CAPACITORS <1.0 ARE IN µf, >1.0 ARE IN pf
4. ALL RESISTORS ARE IN Ω; 1/4W, 5%
5. ☐ 7085-1 TO 7085-2 PCB INTERCONNECT
6. ▭ DENOTES FRONT PANEL WORDING.

REF. PCB 7085-1A

R1	R10	
S1	S36	
Q1	Q1	
Z1	Z14	
DS1	DS20	
C1	C3	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

BNC BERKELEY NUCLEONICS CORP. 1198 TENTH ST., BERKELEY, CA 94710

SCALE	APPROVED BY	DRAWN BY G.T.
DATE 3-20-79		REVISED

DIGITAL DELAY GENERATOR MODEL 7085

DISPLAY CIRCUITS — D — DRAWING NUMBER 7085-30

REVISIONS			
LTR	DATE	DESCRIPTION	BY

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL CAP. <1.0 ARE IN μF AND >1.0 ARE IN pF.
2. ALL RESISTORS ARE IN Ω, 1/4W, 5%.
3. □ DENOTES 7085-1 TO 7085-2 PCB INTERCONNECT.
4. IC'S 7400, 7404, 7408, 7420, 7414, 7430 HAVE PIN 7=GND, PIN 14=+5V.

REF. PCB 7085-2A

CR1	CR3
Z1	Z24
C1	C5
R1	R37

FIRST LAST OMITTED

REFERENCE DESIGNATIONS

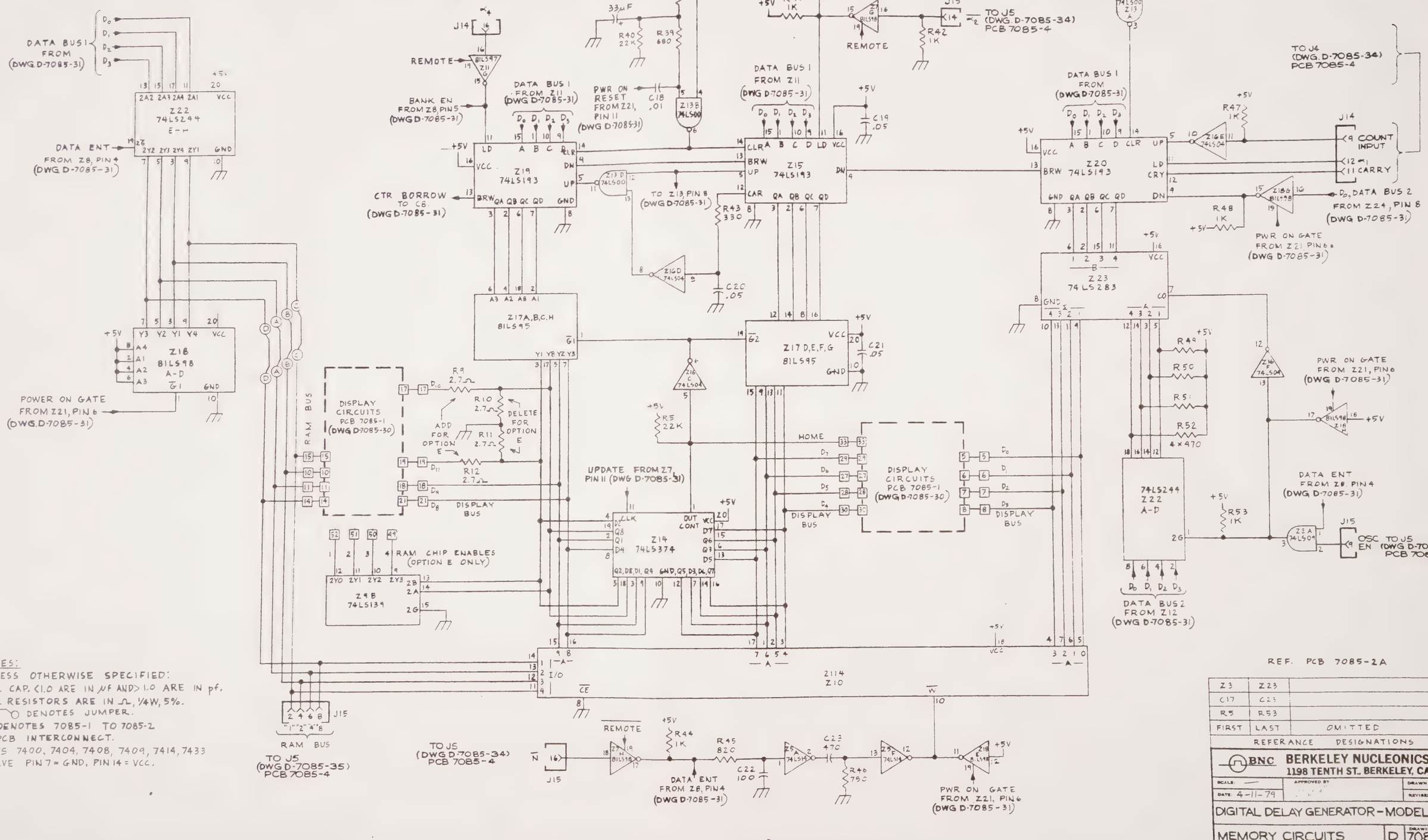
BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE	APPROVED BY	DRAWN BY
DATE: 4-4-72		REVISED

DIGITAL DELAY GENERATOR MODEL 7085

DATA ENTRY CIRCUITS | D | DRAWING NUMBER 7085-31

REVISION		
LTR	DATE	DESCRIPTION
A	5-80	PER ECO 80-044


DATA BUS 1 FROM (DWG D-7085-31)
Z22 74LS244 E-H
DATA ENT FROM Z8, PIN 4 (DWG D-7085-31)
Z18 BIL598 A-D
POWER ON GATE FROM Z21, PIN 6 (DWG D-7085-31)
RESET FROM Z9, PIN 4 (DWG D-7085-31)
TO J4 (DWG D-7085-34) PCB 7085-4
REMOTE
BANK EN FROM Z8, PIN 5 (DWG D-7085-31)
DATA BUS 1 FROM Z11 (DWG D-7085-31)
PWR ON RESET FROM Z21, PIN 11 (DWG D-7085-31)
Z19 74LS193
CTR BORROW TO C8. (DWG D-7085-31)
Z17A,B,C,H BIL595
Z15 74LS193
TO Z13, PIN 8 (DWG D-7085-31)
REGIS EN. FROM Z8, PIN 6 (DWG D-7085-31)
Z17 D,E,F,G BIL595
DISPLAY CIRCUITS PCB 7085-1 (DWG D-7085-30)
RAM BUS
ADD FOR OPTION E
DELETE FOR OPTION E
DISPLAY BUS
UPDATE FROM Z7, PIN 11 (DWG D-7085-31)
Z14 74LS374
HOME
RAM CHIP ENABLES (OPTION E ONLY)
Z9B 74LS139
Z114 Z10
RAM BUS
TO J5 (DWG D-7085-35) PCB 7085-4
TO J5 (DWG D-7085-34) PCB 7085-4
REMOTE
DATA ENT FROM Z8, PIN 4 (DWG D-7085-31)
PWR ON GATE FROM Z21, PIN 6 (DWG D-7085-31)
UPDATE FROM Z7, PIN 11 (DWG D-7085-31)
CTR RESET FROM Z3, PIN 9 (DWG D-7085-31)
DATA BUS 1 FROM (DWG D-7085-31)
Z20 BRW 74LS193
TO J4 (DWG D-7085-34) PCB 7085-4
COUNT INPUT
CARRY
D0, DATA BUS 2 FROM Z24, PIN 8 (DWG D-7085-31)
PWR ON GATE FROM Z21, PIN 8 (DWG D-7085-31)
Z23 74LS283
74LS244 Z22 A-D
DATA BUS 2 FROM Z12 (DWG D-7085-31)
PWR ON GATE FROM Z21, PIN 6 (DWG D-7085-31)
DATA ENT FROM Z8, PIN 4 (DWG D-7085-31)
OSC TO J5 EN (DWG D-7085-3 PCB 7085-4

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL CAP. <1.0 ARE IN μF AND > 1.0 ARE IN pf.
2. ALL RESISTORS ARE IN Ω, 1/4W, 5%.
3. ○⌒○ DENOTES JUMPER.
4. □ DENOTES 7085-1 TO 7085-2 PCB INTERCONNECT.
5. IC'S 7400, 7404, 7408, 7409, 7414, 7433 HAVE PIN 7 = GND, PIN 14 = VCC.

REF. PCB 7085-2A

Z3	Z23	
C17	C23	
R5	R53	
FIRST	LAST	OMITTED

REFERANCE DESIGNATIONS

BNC BERKELEY NUCLEONICS CO
1198 TENTH ST., BERKELEY, CA 94

SCALE:	APPROVED BY	DRAWN BY
DATE: 4-11-79		REVISED

DIGITAL DELAY GENERATOR - MODEL 708

MEMORY CIRCUITS | D | DRAWING NUMBER 7085-3

REVISIONS			
LTR	DATE	DESCRIPTION	BY

J901
SHIELD 12
GND 24
LOGIC
PROGRAM IN
EOI 5
REN 17
DATA BUS: DIO8 16, DIO1 1, DIO2 2, DIO3 3, DIO4 4, DIO5 13, DIO6 14, DIO7 15
TRANSFER CONTROL: DAV6 6, NDAC 8, NRFD 7
GND 18, GND 19, GND 20, GND 21, GND 22, GND 23
INTERFACE MANAGE: ATN 11, IFC 9, SRQ 10
ERROR OUT
FROM J2 PCB 7085-1 (DWG. D-7085-40)
TO J2 PCB 7085-1 (DWG. D-7085-40)
J12: ERROR 7, RESET 10, RESET 8

R1 3K TYP.
R1 6.2K TYP.
R2 4.7K
R3 10K
R4 2.7K
R5 1.5K
R6 560
R7 1.5K
R9 1.5K
R10 560
R11 560
R12 22K
R13 1.5K
R14 3.3K
R15 6.8K
R16 2.2K
R17 1.5K
R18 1K
R19 1.5K
R20 2.2K
R22 22K TYP.
R23 1.5K
C1 330pF
C2 270
C3 .05
C4 .05
C5 100
C6 6.8µF
C7 6.8µF
C8 .05
C9 33µF
CR1 IN270
CR2 IN270
CR3 IN270
CR4 IN270
DS1 ADDR
DS2 RE
Q1 2N3646
Z25 8136 COMP.
Z15 74LS138
Z25A 74LS107
Z25B 74LS107
Z1A 74LS32
Z1B 74LS38
Z1C 74LS38
Z1D 74LS38
Z2A 74LS33
Z2B 74LS33
Z2C 74LS33
Z2D 74LS33
Z3A 74LS03
Z3B 74LS03
Z3C 74LS03
Z3D 74LS03
Z4A 74LS33
Z4B 74LS33
Z4C 74LS32
Z4D 74LS32
Z6 LS05
Z7 LS14
Z8A 7438
Z8B 7438
Z8C 7438
Z8D 7438
Z14A 74LS32
Z14B 74LS32
Z14C 74LS32
Z14D 74LS32
SIA, SIB, SIC, SID, SIE
ADRS (SELECT GND="1")
OFF / ON
RESET MODE: NORM / SIF / RESET
SIG AFTER / DURING

J4
10 DO, 3 DI, 13 D2, 14 D3 — DATA BUS1
FROM J14 (DWG. D-7085-31) PCB 7085-2
15 =3
1 REM EN
2 GND, 4 GND, 5 GND, 6 GND, 7 GND, 8 GND
16 =4
FROM J14 (DWG. D-7085-32) PCB 7085-2
9 COUNT OUTPUT
12 =1
11 CARRY
J5
14 =2
16 N
9 OSC EN
12 =1
15 REM
13 UPDATE
FROM J15 (DWG. D-7085-32) PCB 7085-2
1 GND, 3 GND, 7 GND, 10 GND
FROM J15 (DWG. D-7085-31) PCB 7085-2
TO PIN 8 OF Z1, Z2, Z3, Z4, Z9, Z17, Z18 & Z19
TO PIN 9 OF Z1, Z2, Z3, Z4, Z9, Z17, Z18 & Z19
REFERENCE (DWG. D-7085-35)

NOTES:
UNLESS SPECIFIED OTHERWISE:
1. RESISTORS ARE 1/4W, 5%
2. * & ** DIP NETWORK R1. *** SIP NETWORK R22.
3. CAPACITORS; VALUES < 1.0 ARE IN µF ; VALUES > 1.0 ARE IN pF
4. IC'S; PIN 14 TO +5V; PIN 7 TO GND. FOR Z6, Z7, Z8, Z14, Z23 & Z24.
5. DENOTES REAR PANEL WORDING.

LAST USED	OMITTED
C21	C1
CR4	
DS2	
Q1	
R23	R21
S1	
Z25	

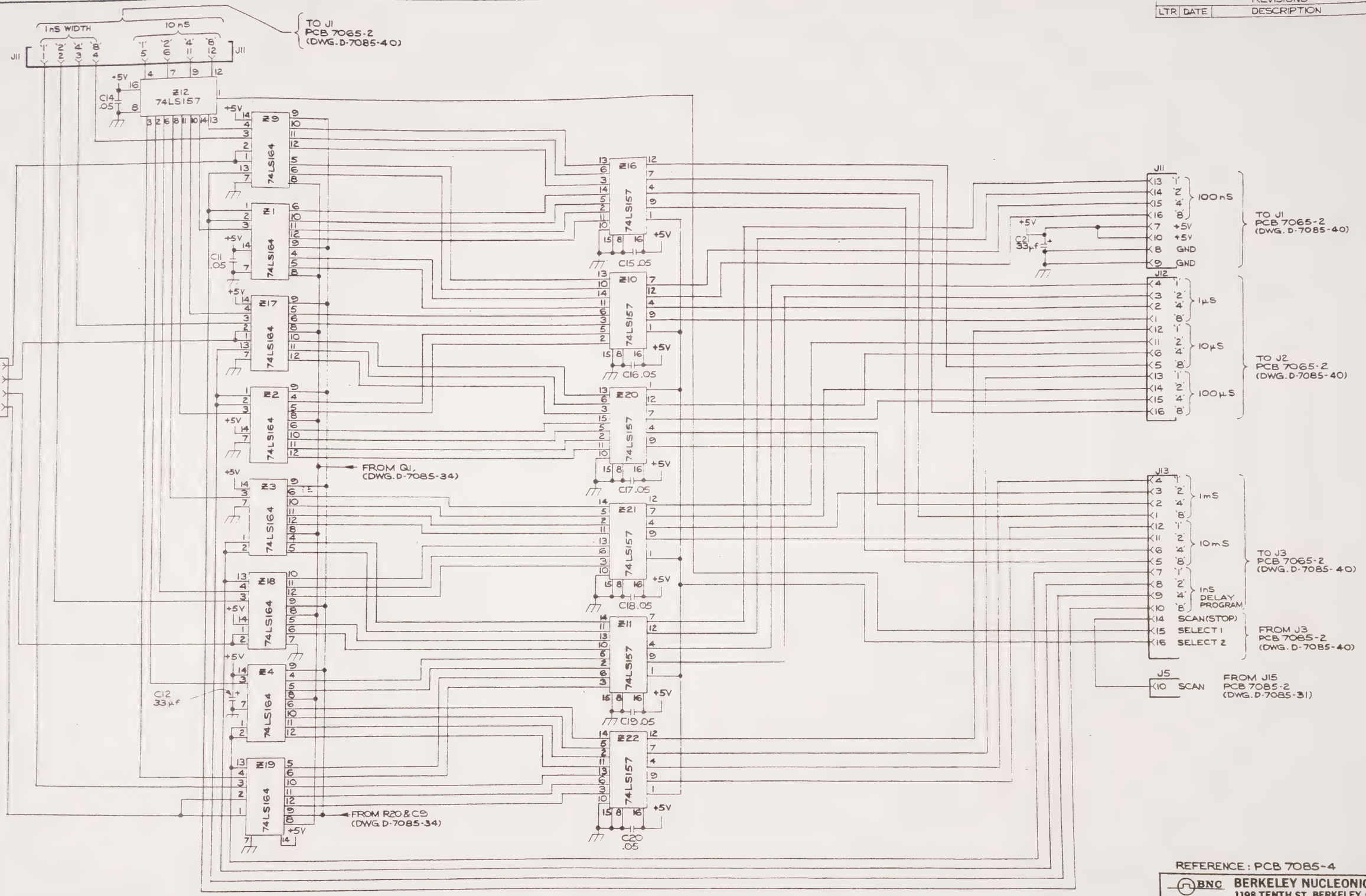
REFERENCE: PCB 7085-4

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE NA	APPROVED BY	DRAWN BY
DATE 21 FEB 80		REVISED

TIMING GENERATOR MODEL 7085
IEEE INTERFACE
D 7085-34

REVISIONS			
LTR	DATE	DESCRIPTION	BY



NOTE:

1. FOR NOTES AND REFERENCE DESIGNATIONS SEE BNC DWG. 7085-34

REFERENCE: PCB 7085-4

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: NA	APPROVED BY:	DRAWN BY
DATE: 31 JAN 80		REVISED

DIGITAL DELAY/WIDTH GENERATOR, MOD. 7085

MULTIPLEX CIRCUITS | D | DRAWING NUMBER 7085-35

DELAY IN PROGRAM FROM PCB 7065-2 (DWG D-7085-40)

FROM 27 → 4 '1'

FROM 24 → 3 '2'

FROM 25 → 2 '4'

FROM 26 → 1 '8'

'1nS' ADJ

'2nS A' ADJ

'4nS' ADJ

'2nS B' ADJ

TRIGGER FROM 17A PCB 7065-1 (DWG. D-7085-38)

ENABLE TO Z5 PIN 5

DELAYED ENABLE TO Z8 PIN 6, Z9 PIN 12

DL1 1nS

DL2 2nS

DL3 4nS

DL4 2nS

DL5 16nS (10')

OSCILLATOR TRIGGER TO 178 PCB 7065-1 (DWG. D-7085-38)

DELAY DRIVE FROM PCB 7065-2 (DWG D-7085-39) 13 POS 14 NEG.

GATE DRIVE FROM PCB 7065-2 (DWG. D-7085-39) 15 NEG 16 POS

SCAN TO 28 PCB 7065-2C (DWG. D-7085-40)

Z3, PIN 1, V_{BB}

DELAYED ENABLE FROM 28

ENABLE FROM 16

DELAYED TRIGGER FROM 21 PCB 7065-1 (DWG. D-7085-38)

COINCIDENCE FROM 23 PCB 7065-2 (DWG. D-7085-39)

CLOCK FROM 15 PCB 7065-1 (DWG. D-7085-38)

DISABLE FROM 8 PCB 7065-2 (DWG. D-7085-39)

NORM → POS. TO 1, NEG. TO 2

COMP → NEG. TO 4, POS. TO 3

INIT → POS TO 9, NEG TO 10

TO PCB 7065-3 (DWG. D-7085-41)

SELECT 2 TO 30 PCB 7065-2C (DWG. D-7085-40)

SELECT 1 TO 29 PCB 7065-2C (DWG. D-7085-40)

TRIGGER IN TO 7 PCB 7065-2 (DWG. D-7085-39)

BUSY GATE TO 31 PCB 7065-1 (DWG. D-7085-37)

NOTES:

1. ALL RESISTORS; ¼W, 5%, UNLESS SPECIFIED OTHERWISE.
2. CAPACITORS WITH VALUES >0 ARE IN pf, <0 ARE IN µf, UNLESS SPECIFIED OTHERWISE.
3. POWER CONNECTIONS SHOWN IN TABLE I.
4. XX INDICATES TWISTED PAIR.
5. □ INDICATES PCB CONNECTIONS.
6. * INDICATES A 5 RESISTOR NETWORK IN A 6 PIN SIP.
7. ** INDICATES LONG LEAD IN TEFLON SLEEVE.
8. ALL ECL CHIPS HAVE .01µf CAPACITOR FROM PIN 8 TO GND.

TABLE 1

IC	PIN # GND	PIN # +5V	PIN # -5V
Z1	7	14	
Z2	16	9	8
Z3		9	8
Z4, Z5, Z7, Z9	1, 16		8
Z6, Z8, Z10, Z11	1, 16		8
Z12	3, 5	4 +12	11 -12

TABLE 2

FIRST	LAST	OMITTED
C1	C32	
CR1	CR2	
L1	L4	
Q1	Q1	
R1	R64	
TPA	TPA	
Z1 — Z12		

REF. PCB 7085-5A

BNC BERKELEY NUCLEONICS CORP. 1198 TENTH ST., BERKELEY, CA 94710

SCALE NA | APPROVED BY | DRAWN BY

DATE 24 MAR. 80 | REVISED

DIGITAL DELAY GENERATOR MOD. 7085

MULTIPLEX CONTROL CKT | D | DRAWING NUMBER 7085-36

REVISIONS			
LTR	DATE	DESCRIPTION	BY

POWER INPUT

-5V → 26 → C45 .01, C46 .01, C47 .01, C48 .01, C49 .01, C50 .01, C51 .01, C52 .01; C55 .01, C56 .01, C57 .01, C58 .01, C59 .01, C60 .01, C61 .01, C62 .01, C63 .01, C54 33µF → -5V(A)

-5V → 5 → C64 .01, C65 .01, C68 33µF → -5V(B)

+5V → 2 → C66 .01, C67 .01, C69 33µF → +5V(A)

+5V → 7 → C70 33µF → +5V(B)

-12V → 8 → -12V

+12V → 9 → +12V

GND → 30

MANUAL TRIGGER GENERATOR

MANUAL, S802, R71 220, R131 220, Z2A 10102, Z2B 10102, Z2C 10102, Z2D 10102, R54 1K, R55 150, C22 22, R56 1K, R57 1K, R58 390

EXTERNAL TRIGGER CIRCUITS

EXT TRIG INPUT, J801, 18, R68 56 1/2W, R69 390, R70 91, Z7 6B5, C26 .01, C25 .01, +5V(A), -5V(A)

EXT TRIG LEVEL, 29, R801 500, 28, CW, 19, R72 1.2K, R73 15K, R74 3.3K, R75 120, C71 .01

Z3A 10102, Z3B 10212, Z4A 10106, Z4B 10106, Z4C .0106, Z3C 10102, Z3D 10102, Z8A 10212, Z8B 10212

R79 390, R80 220, C28 33, R81 390, R76 220, C29 33

OSCILLATOR STOP SIGNAL TO 17A PCB 7085-1 (DWG. D-7085-38)

ERROR DETECTION CIRCUITS

R78 47, R77 47, CR11 IN4152, CR12 IN4152, CR10 IN4152, CR9 IN4152

SLOPE, S801, 14, 15, +, -

R82 10K, C30 .01, R83 10K, C31 .01, R84 390, C32 33, R86 390, C33 99, R87 1K

31, BUSY GATE FROM 26 PCB 7085-5 (DWG D-7085-36)

R85 1K, R111 10, CR14 IN270, Q6 2N3640, R112 56

10, ERROR SIGNAL TO 4 PCB 7065-2 (DWG. D-7085-40)

10, ERROR SIGNAL FROM EXT REF CKTS; 15 PCB 7065-6 (DWG. D-7085-44) OPTION B ONLY

DS801, ERROR

R110 1K, R105 27K, R107 1K, C42 22, R106 1K, R108 1.8K, C43 33µF, R109 1K, CR13 IN270

TRIGGER MODE

S803A, CR802 IN4152, CW, 20, 22, R59 10K, Z22B 10116, FINE, R60 430, 25, R802 10K, 24, 23, C23 100, Z22A 10116, R62 1K, C53 10, R66 68, R64 150, R63 1K, R65 1.5K, C24 100, Z22C 10116, R67 390

MANUAL, S803B, CW, EXT TRIG, 50 Hz, C801, 10, 500 Hz, C802, 1, 5 kHz, C803, .1, 50 kHz, C804, .01, 500 kHz, C805, .001, 5 MHz

INTERNAL TRIGGER GENERATOR

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4W, 5%
   ALL CAPACITORS < 1.0 ARE IN µF AND > 1.0 ARE IN pF.
2. IC POWER AND GROUND CONNECTIONS NOT ON SCHEMATIC ARE LISTED IN TABLE 1.
3. ●— DENOTES PCB TEST POINT
4. □ DENOTES PCB WIRING CONNECTIONS
5. ▭ DENOTES FRONT PANEL NOMENCLATURE.
6. ⟩⟨ TWISTED PAIR TRANSMISSION LINES
7. ALL COMPONENTS CARRYING "800" SERIES NO'S ARE LOCATED ON FRONT PANEL AND ARE REF. ONLY.

TABLE 1

IC POWER & GROUND CONNECTIONS			
I C NO.	GND PIN	PWR PIN	PWR SOURCE
Z8	1, 15, 16	8	-5V (A)
Z2-Z4 Z22	1, 16	8	-5V (A)

Z1	Z25	Z26
Y1	Y1	
T1	T1	
FIRST	LAST	OMITTED
REFERENCE DESIGNATIONS (CONT.)		

REF. PCB 7065-1D

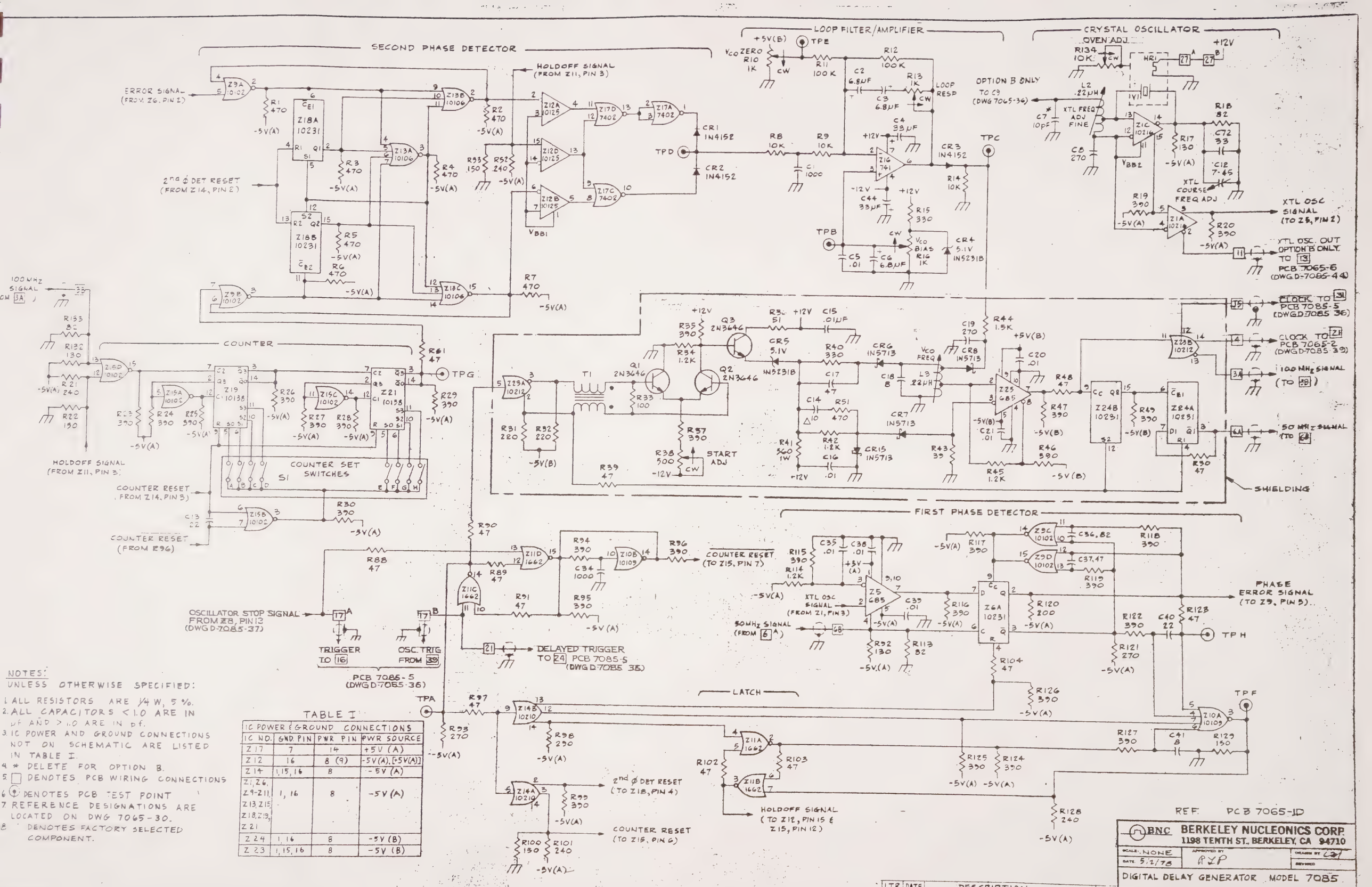
TPA	TPF	
S	S	
R1	R34	R61-R127
Q1	Q6	
L1	L4	
J801	J801	
HR1	HR1	
DS801	DS801	
DL1	DL1	
CR1	CR15	
C1	C72	C44,
FIRST	LAST	OMITTED
REFERENCE DESIGNATIONS		

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE NONE	APPROVED BY RLP	DRAWN BY LJH	
DATE 5/9/78		REVISED	

DIGITAL DELAY GENERATORS, MODEL 7085

INPUT CIRCUITS | D | DRAWING NUMBER 7085-37



NOTES:
UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE ¼ W, 5 %.
2. ALL CAPACITORS < 1.0 ARE IN pF AND > 1.0 ARE IN µf.
3. IC POWER AND GROUND CONNECTIONS NOT ON SCHEMATIC ARE LISTED IN TABLE I.
4. * DELETE FOR OPTION B.
5. □ DENOTES PCB WIRING CONNECTIONS
6. ⊙ DENOTES PCB TEST POINT
7. REFERENCE DESIGNATIONS ARE LOCATED ON DWG 7065-30.
8. ' DENOTES FACTORY SELECTED COMPONENT.

TABLE I

IC POWER & GROUND CONNECTIONS			
IC NO.	GND PIN	PWR PIN	PWR SOURCE
Z 17	7	14	+5V (A)
Z 12	16	8 (9)	-5V(A), [-5V(A)]
Z 14	1, 15, 16	8	-5V (A)
Z1, Z6, Z9-Z11, Z13, Z15, Z18, Z19, Z 21	1, 16	8	-5V (A)
Z 24	1, 16	8	-5V (B)
Z 23	1, 15, 16	8	-5V (B)

REF: PCB 7065-1D

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: NONE | APPROVED BY: RVP | DRAWN BY: CJ
DATE: 5/2/78 | REVISED

DIGITAL DELAY GENERATOR MODEL 7085

CLOCK SYNCHRONIZING CKT'D | DRAWING NUMBER: 7085-3B

LTR	DATE	DESCRIPTION	BY
		REVISIONS	

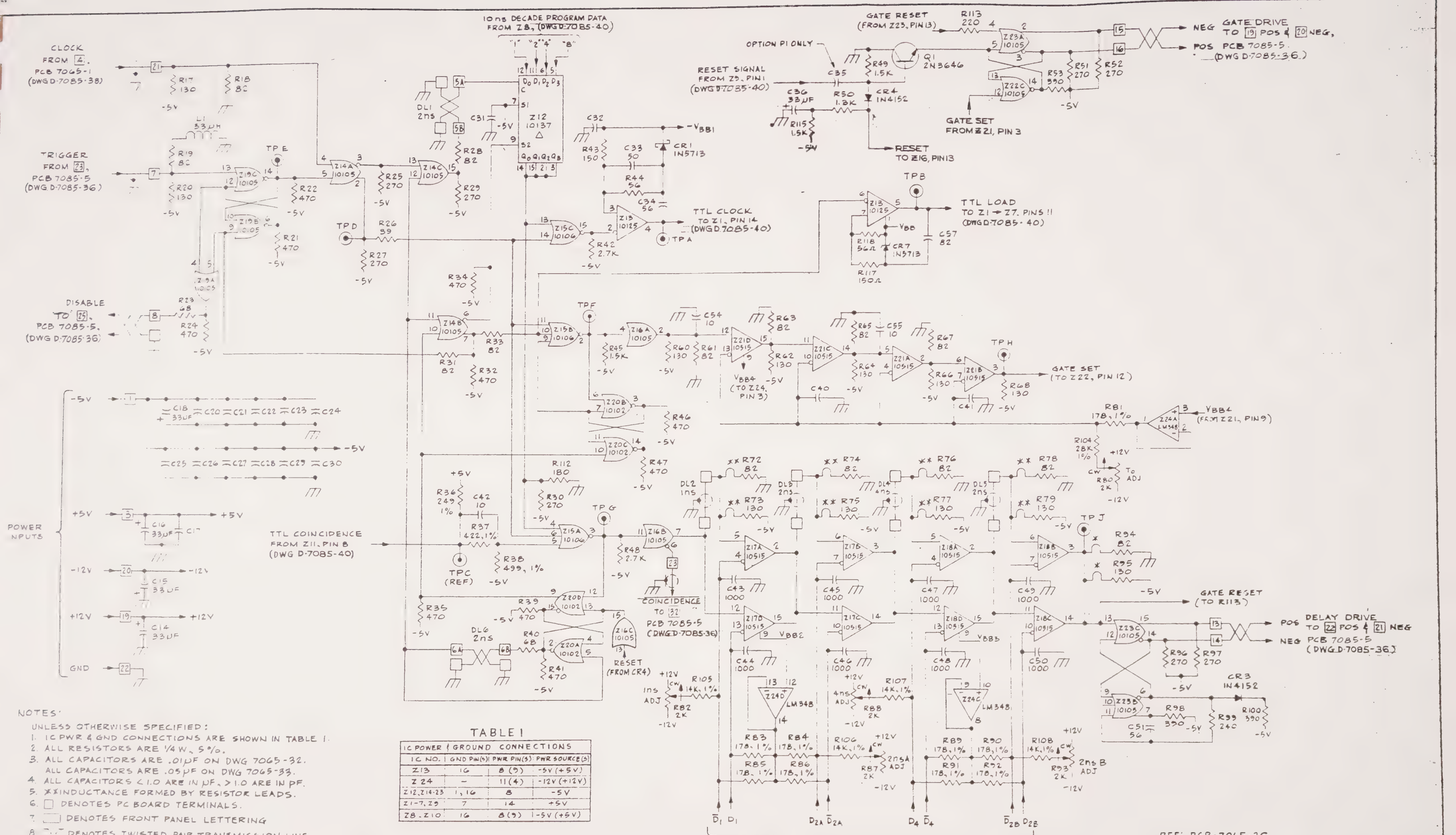

10 ns DECADE PROGRAM DATA FROM Z8, (DWG D-7085-40)
"1" "2" "4" "8"
CLOCK FROM 4, PCB 7065-1 (DWG D-7085-38)
TRIGGER FROM 23, PCB 7085-5 (DWG D-7085-36)
DISABLE TO 25, PCB 7085-5, (DWG D-7085-36)
GATE RESET (FROM Z23, PIN 13)
OPTION P1 ONLY
RESET SIGNAL FROM Z9, PIN 1 (DWG D-7085-40)
GATE SET FROM Z1, PIN 3
RESET TO Z16, PIN 13
NEG GATE DRIVE TO 19 POS & 20 NEG,
POS PCB 7085-5 (DWG D-7085-36)
TTL CLOCK TO Z1, PIN 14 (DWG D-7085-40)
TTL LOAD TO Z1 → Z7, PINS 11 (DWG D-7085-40)
GATE SET (TO Z22, PIN 12)
VBB4 (TO Z24, PIN 3)
VBB1
VBB2
VBB3
VBB4 (FROM Z21, PIN 9)
+12V
To ADJ
TTL COINCIDENCE FROM Z11, PIN 8 (DWG D-7085-40)
COINCIDENCE TO 32 PCB 7085-5 (DWG D-7085-36)
RESET (FROM CR4)
GATE RESET (TO R113)
POS DELAY DRIVE TO 22 POS & 21 NEG
NEG PCB 7085-5 (DWG D-7085-36)
POWER INPUTS
+5V
-12V
+12V
GND
1ns DECADE PROGRAM DATA FROM Z10 (DWG D-7085-40)
D1 D1 D2A D2A D4 D4 D2B D2B
REF: PCB-7065-2C

TABLE I

IC POWER & GROUND CONNECTIONS			
IC NO.	GND PIN(S)	PWR PIN(S)	PWR SOURCE(S)
Z13	16	8 (9)	-5V (+5V)
Z 24	–	11(4)	-12V (+12V)
Z12, Z14-23	1, 16	8	-5V
Z1-7, Z9	7	14	+5V
Z8, Z10	16	8 (9)	-5V (+5V)

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. IC PWR & GND CONNECTIONS ARE SHOWN IN TABLE I.
2. ALL RESISTORS ARE 1/4 W, 5%.
3. ALL CAPACITORS ARE .01μF ON DWG 7065-32. ALL CAPACITORS ARE .05μF ON DWG 7065-33.
4. ALL CAPACITORS < 1.0 ARE IN μF, > 1.0 ARE IN PF.
5. **INDUCTANCE FORMED BY RESISTOR LEADS.
6. □ DENOTES PC BOARD TERMINALS.
7. ▭ DENOTES FRONT PANEL LETTERING
8. ⌒ DENOTES TWISTED PAIR TRANSMISSION LINE.
9. ⊙ DENOTES TEST POINT.
10. REFERENCE DESIGNATIONS ARE ON DWG NO 7065-33
11. △ DENOTES HEAT SINK ON COMPONENT.

BNC BERKELEY NUCLEONICS CORP.
2198 TENTH ST. BERKELEY, CA 94710

SCALE	APPROVED BY	DRAWN BY
DATE 3-30-79	RLP	REVISED

DIGITAL DELAY GENERATOR MODEL 7085

TIMING CIRCUITS (ECL) D 7085-32

REVISIONS			
LTR	DATE	DESCRIPTION	BY

ERROR SIGNAL FROM ID PCB 7065-1 (DWG D-7085-37)

R12 3.3K, R13 82, C13, CR5 IN4152, +5V, -5V, Z9B 7400

J2 ERROR SIGNAL TO J12 PCB 7085-4 (DWG D-7085-34)

REMOTE RESET FROM J12 PCB 7085-4 (DWG D-7085-34)

J2 10 RESET, 8 RESET

R.E 22K, R.F 22K, Z9A 7400

RESET SIGNAL TO C35 (DWG D-7085-39)

DATA INPUT

FROM J11 PCB 7085-4 (DWG D-7085-35)

FROM J12 PCB 7085-4 (DWG D-7085-35)

FROM J13 PCB 7085-4 (DWG D-7085-35)

TO J13 PCB 7085-4 (DWG D-7085-35)

FROM J13 PCB 7085-4 (DWG D-7085-35)

J1 100 nS WIDTH 4 3 2 1 7 10 — 10 NS 12 11 6 5 8 9 — 100NS 13 14 15 16 J1

J2 1μS 4 3 2 1 — 10μS 12 11 6 5 — 100μS 13 14 15 16 J2

J3 1mS 4 3 2 1 — 10mS 12 11 6 5 — SEL1 15, SEL2 16, SCAN 14 — 1nS DELAY PROGRAM 1 2 4 8 — 7 8 9 10 J3

R1 22K, R2 22K, R3 22K, R4 22K, R5 22K, R6 22K, R7 22K, R8 22K, +5V, -5V

R.C 10K, R.E 2K, R.F 2K, R111 1K, R.C 1K, R.D 1K, R.G 1K

Z8A 10124, Z8B 10124, Z8C 10124, Z8D 10124, Z10B 10124, Z10C 10124, Z10D 10124, Z9C 7404, Z9D 7404

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C56 C57

TPA, TPB, TPC

Z1 74190 (A B C D, DN/UP, LOAD, CL, EN, GND, M/M, R_x, V_{cc}), Z2 74190, Z3 74190, Z4 74190, Z5 74190, Z6 74190C

RGE 22K

R116 1K, Q5 2N3646, C56 10pf, R114 2.2K

Z11 7453C, R9 22K

CR6 IN4152

TTL LOAD FROM Z13 PIN 5 (DWG D-7085-39)

TTL CLOCK FROM Z13 PIN 4 (DWG D-7085-39)

TTL COINCIDENCE TO CR6 (DWG D-7085-39)

27 24 25 26 — 4 3 2 1 — TO 1nS DELAY PROGRAM PCB 7085-5 (DWG D-7085-36)

28 SCAN FROM 7 PCB 7085-5 (DWG D-7085-36)

30 SELECT 2 FROM 8 PCB 7085-5 (DWG D-7085-36)

29 SELECT 1 FROM 9 PCB 7085-5 (DWG D-7085-36)

D2B $\overline{D_{2B}}$ D4 $\overline{D_4}$ D2A $\overline{D_{2A}}$ D1 $\overline{D_1}$

1 NS DECADE PROGRAM DATA TO Z17 & Z18 (DWG D-7085-39)

8 4 2 1

10 NS DECADE PROGRAM DATA TO Z12 (DWG D-7085-39)

ECL DECODERS

TTL COINCIDENCE CIRCUIT

TTL COUNTERS

NOTE:
1. SEE DWG. 7085-39 FOR NOTES & POWER CONNECTION TABLE.

REFERENCE: PCB 7065-2C

TPA	TPJ	TPI
R804	R806	R805
R1	R117	
Q1	Q5	
L1	L1	
J1	J3	
DL1	DL6	
CR1	CR6	C11
C1	C56	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

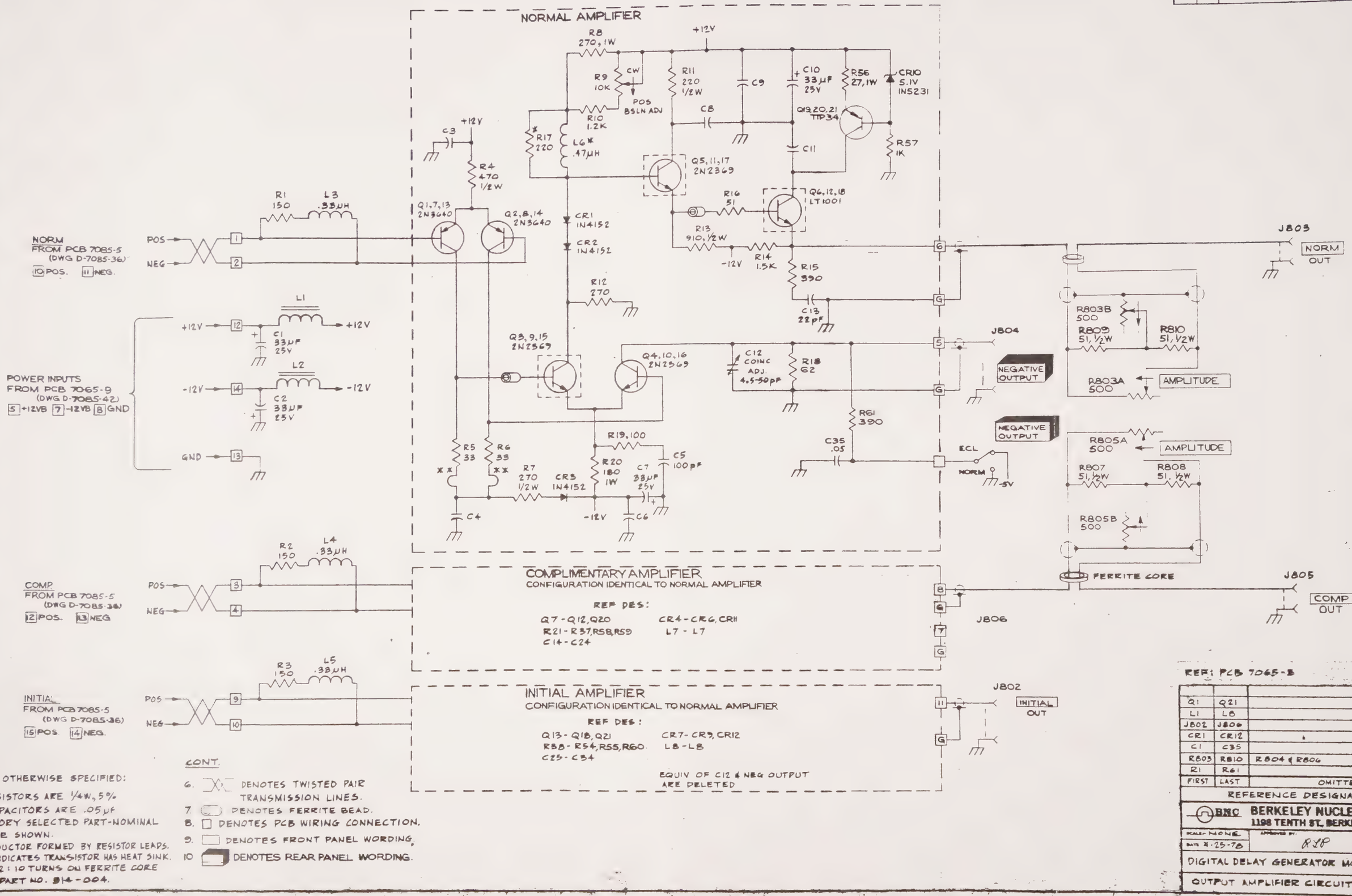
BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: ~ | APPROVED BY: RLP | DRAWN BY: | REVISED:
DATE: 4/20/78

DIGITAL DELAY GENERATOR MODEL 7085

TIMING CIRCUITS, TTL | D | 7085-40

REVISIONS			
LTR	DATE	DESCRIPTION	BY



NOTES:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W, 5%
ALL CAPACITORS ARE .05µF
FACTORY SELECTED PART-NOMINAL VALUE SHOWN.
* INDUCTOR FORMED BY RESISTOR LEADS.
- - - INDICATES TRANSISTOR HAS HEAT SINK.
L1 & L2: 10 TURNS ON FERRITE CORE BNC PART NO. 914-004.

CONT.
6. DENOTES TWISTED PAIR TRANSMISSION LINES.
7. DENOTES FERRITE BEAD.
8. DENOTES PCB WIRING CONNECTION.
9. DENOTES FRONT PANEL WORDING.
10. DENOTES REAR PANEL WORDING.

REF: PCB 7065-B

Q1	Q21	
L1	L8	
J802	J806	
CR1	CR12	
C1	C35	
R803	R810	R804 & R806
R1	R61	
FIRST	LAST	OMITTED

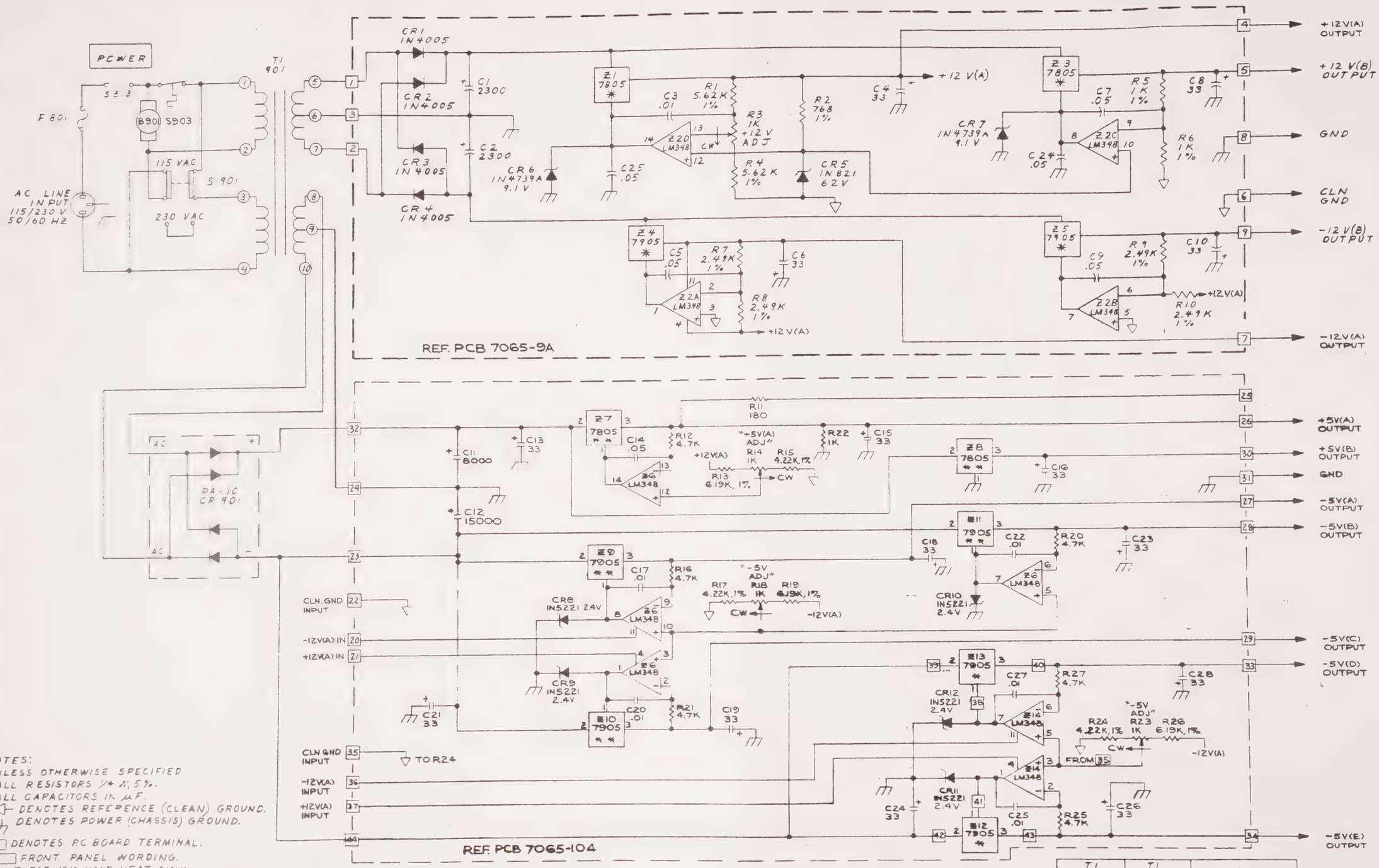
REFERENCE DESIGNATIONS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST, BERKELEY, CA 94710

SCALE: NONE	APPROVED BY: RLP	DRAWN BY: LJK
DATE 11-25-78		

DIGITAL DELAY GENERATOR MODEL 7085

OUTPUT AMPLIFIER CIRCUITS D 7085-41



NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ¼ W, 5%.
2. ALL CAPACITORS IN μF.
3. ◁ DENOTES REFERENCE (CLEAN) GROUND.
4. ⏚ DENOTES POWER (CHASSIS) GROUND.
5. □ DENOTES P.C. BOARD TERMINAL.
6. ▭ FRONT PANEL WORDING.
7. ✳ THESE IC'S HAVE HEAT SINK.
8. ✳ ✳ THESE IC'S MOUNTED TO HEAT SINK, REAR PANEL.

T1	T1	
B901	B901	
SB13, S901	SB13, S903	S902
F801	F801	
Z1	Z14	
CR1, CR901	CR12, CR901	
C1	C28	
R1	R27	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

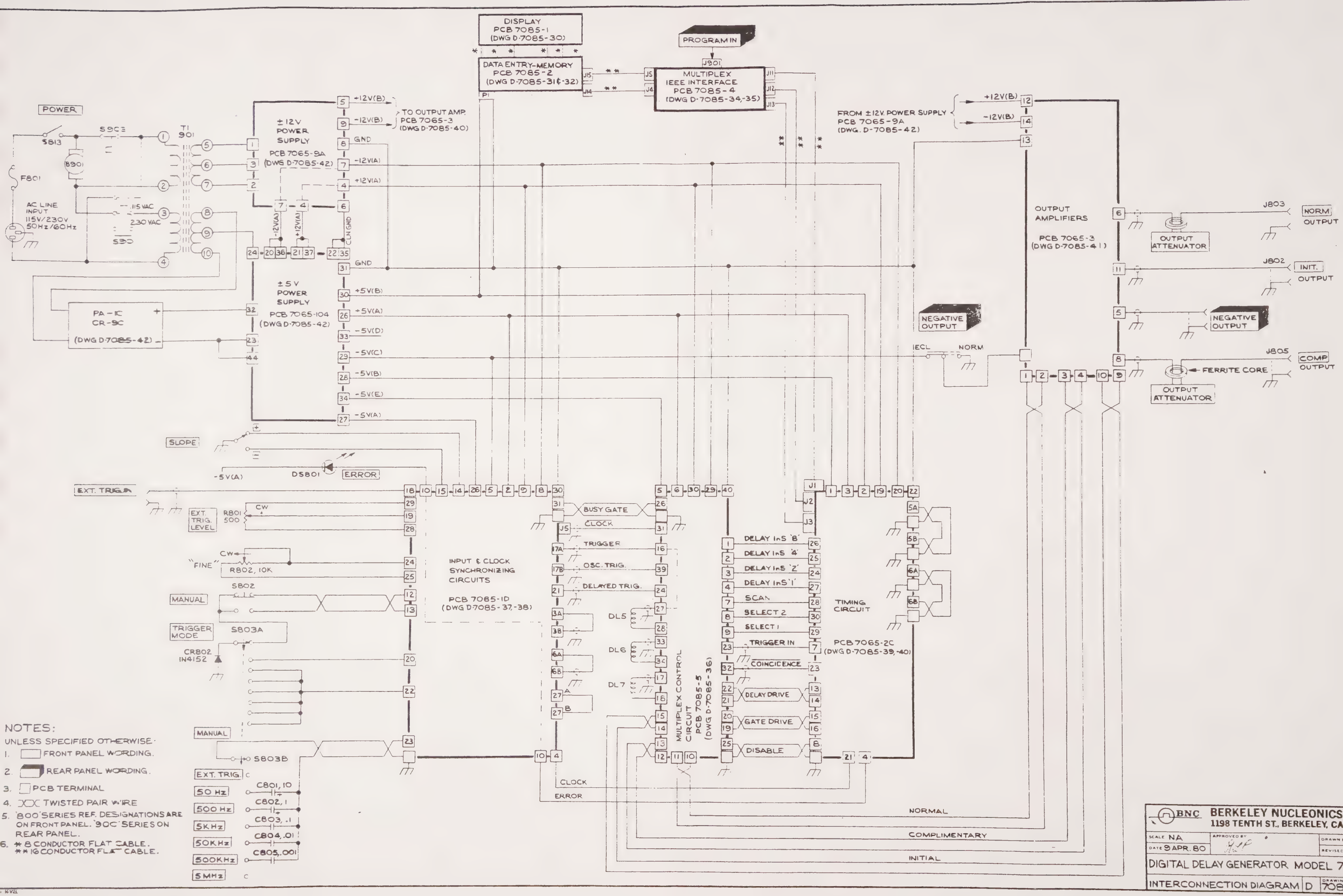
LTR	DATE	DESCRIPTION	BY
REVISION BLOCK			

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: —	APPROVED BY:	DRAWN BY: G.J.
DATE: 10-30-78		REVISED:

DIGITAL DELAY GENERATOR MODEL 7085

POWER SUPPLY | D | 7085-42



NOTES:
UNLESS SPECIFIED OTHERWISE.

1. ▭ FRONT PANEL WORDING.
2. ▭ REAR PANEL WORDING.
3. ▭ PCB TERMINAL
4. XXX TWISTED PAIR WIRE
5. '800' SERIES REF. DESIGNATIONS ARE ON FRONT PANEL. '90C' SERIES ON REAR PANEL.
6. * 8 CONDUCTOR FLAT CABLE. ** 16 CONDUCTOR FLAT CABLE.

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE NA	APPROVED BY	DRAWN BY	
DATE 9 APR. 80		REVISED	

DIGITAL DELAY GENERATOR MODEL 7085

INTERCONNECTION DIAGRAM | D | DRAWING NUMBER 7085-43

REVISIONS			
LTR.	DATE	DESCRIPTION	BY

PHASE DETECTOR / LOOP FILTER

OUT OF LOCK DETECTOR

INPUT CKTS

EXT. REF. INPUT
1MHz OR 10MHz

J902

TO SIGNAL DETECTOR, (C13)

S902 10 MHz / 1 MHz

XTL OSC INPUT FROM [11] PCB 7065-1, (DWG.D-7085-38)

TPA TPB TPC TPD TPE

Z1A 74132 Z1B 74132 Z1C 74132 Z1D 74132

Z2 74190

Z3 4044

Z4 10138

Z6 10138

Z5A 10102 Z5B 10102 Z5C 10102 Z5D 10102

Z7 741

Q1 MPS 6534 Q2 MPS6534 Q3 2N 3646 Q4 MPS 6531 Q5 MPS 6531

CR1 CR2 CR3 CR4 CR5 CR6 CR7 IN5231 CR8 IN5231 CR9 CR10 CR11 CR12

C1 100 C2 .05 C3 .05 C4 250 C5 .01 C6 33 µF C7 .05 C8 .05 C9 .001 C10 .05 C11 .05 C12 18 C13 250 C14 .01 C15 6.8µF

C9 20 C10 270 C11 270

L1 5.6 µH

R1 150 R2 22K R3 22K R4 3.9K R5 6.8K R6 3.3K R7 1.5K R8 390 R9 220 R10 1K R11 82 R12 390 R13 390 R14 130 R15 82 R16 390 R17 390 R18 390 R19 390 R20 390 R21 390 R22 390 R23 3.9K R24 47K R25 10K R26 10K R27 4.7K R28 6.8K R29 10K R30 1K R31 10K R32 100K R33 100 R34 10K R35 10K R36 500 POS. LIMIT SET R37 500 NEG. LIMIT SET R38 3.3K R39 56K R40 3.3K R41 84 ½W R42 470 R43 470

+5V +12V -12V -5V

ERROR SIGNAL TO [10], PCB 7065-1 (DWG.D-7085-37)

VXCO CONTROL TO CRYSTAL OSCILLATOR (L2)

VXCO SET

ADDED TO CLOCK SYNC CKT BD., PCB 7065-1 (DWG. D7085-38) WITH THIS OPTION

DIVIDE BY 101

AMPLIFIER / DRIVER

SIGNAL DETECTOR

SIGNAL DETECTOR IN PUT (FROM Z10, PIN 11)

POWER INPUTS

C16 33µF, 25V

C17 33µF, 25V

C18 33µF, 25V

C19 33µF, 25V

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ¼ W, 5%
2. ALL CAPS. > 0 IN PF, < 0 IN µF
3. ▭ REAR PANEL NOMENCLATURE
4. Z5, 10102 GND = PINS 1, 16; -5V = PIN 8
5. Z1, 74132, GND = PINS 7, +5V = PIN 14
6. ALL DIODES - IN4152
7. □ DENOTES PCB WIRING CONNECTIONS.
8. ⊙— DENOTES TEST POINT

REF: PCB 7065-6

TPA	TPE	
CR1	CR12	
Q1	Q4	
Z1	Z7	
C1	C19	
R1	R43	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: —
DATE: 11-28-78
APPROVED BY: R.L.P.
DRAWN BY:
REVISED:

DIGITAL DELAY GENERATOR
MODEL 7085 OPTION B

EXTERNAL REFER. CIRCUITS | D | 7085-44

80851

MP MASTER
MA31866